Innovative Power Conditioning and Interfacing Circuitry for various Energy Harvesting Devices

Francarl Galea

Department of Microelectronics and Nanoelectronics
University of Malta
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"Investing in human capital to create more opportunities and promote the well-being of society".

Dedicated to my wife Elise, daughter Elena, and son Matteo.

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Dr. Inġ. Owen Casha

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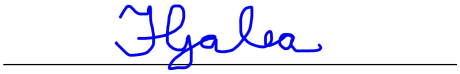
Francarl Galea 

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ABSTRACT

This research work focuses on the design, implementation, fabrication and characterisation of a novel power conditioning integrated circuit proposed for capturing maximal energy from a wide range of energy devices. The proposed power conditioning circuit has a wide input voltage range and power range and employs a maximum power point tracking circuit to operate the energy harvesting device at maximum power at any operating condition. A direct AC/DC-to-DC converter makes this power conditioning circuit compatible with harvesters generating both AC or DC output voltages without the need of external rectification. Energy storage is provided by means of a high storage capacitor which reduces the down time of the load and stores any excess power being generated by the energy harvester. The final stage of the conditioning circuit is a hysteretic controlled buck converter which generates an adjustable, clean, and constant output voltage as required by the load. Both circuit stages were fabricated while requiring a minimum number of external components.

In particular, the work undertaken and explained in this dissertation can be classified into two main parts. The first part focuses on the design, implementation, simulation, fabrication and characterisation of a novel direct AC/DC-to-DC converter with MPPT function.

The second part focuses on the design, implementation, simulation, fabrication and characterisation of a novel hysteretic controlled buck converter integrated with on-chip bootstrapping circuit.

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The fabrication cost of the designed Voltage Regulating Buck Converter, amounting to €12,200, was covered through the Hi-Silicon Sponsorship program. This sponsorship was awarded for the novelty and applicability of the design.

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LIST OF PUBLICATIONS

Portions of the research work presented in this dissertation were published in five peer-reviewed conference proceedings papers and one peer-reviewed journal paper:

1. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "A CMOS MPPT Power Conditioning Circuit for Energy Harvesters," in *2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* pp. 442-445, IEEE, 2017.

2. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "Ultra Low Frequency Low Power CMOS Oscillators for MPPT and Switch Mode Power Supplies," in *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME),* pp. 121-124, IEEE, 2018.

3. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "An Ultra-Low Power CMOS MPPT Power Conditioning Circuit for Energy Harvesters," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 1-5, IEEE, 2020.

4. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "Experimental measurements of a low power CMOS analog MPPT power conditioning circuit for energy harvesting applications," in *European Conference on Electrical Engineering & Computer Science (EECS or ELECS),* 2020.

5. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "Integrated Hysteretic Controlled Regulating Buck Converter with Capacitively Coupled Bootstrapping," in *2021 17th*

Conference on Ph. D. Research in Microelectronics and Electronics (PRIME), pp. 1-4, IEEE, 2021.

6. F. Galea, O. Casha, I. Grech, E. Gatt, and J. Micallef, "Experimental Measurements of an Integrated Hysteretic Controlled Regulating Buck Converter with Capacitively Coupled Bootstrapping," in *2021 28th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* 2021.

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List of Acronyms

1P6M 1-Poly-6-Metal

AC Alternating Current

ADC Analogue to Digital Converter

AMS Austria Microsystems

BCD Bipolar CMOS DMOS

CCM Continuous Conduction Mode

CMOS Complementary Metal-Oxide-Semiconductor

DAC Digital to Analogue Converter

DC Direct Current

DCM Discontinuous Conduction Mode

DRC Design Rule Check

EMF Electromotive Force

GPS Global Positioning System

HV High Voltage

IHP Innovations for High Performance microelectronics

LC Inductance Capacitance

LDR Low Dropout Regulator

MEMS Micro-Electro-Mechanical System

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

MPW Multi-Process Wafer

NMOS Negative channel Metal Oxide Semiconductor

PLECS Piecewise Linear Electrical Circuit Simulation

PMOS Positive channel Metal Oxide Semiconductor

PMU Power Management Unit

PO Perturbation and Observation

PV Photovoltaic

PWM Pulse Width Modulation

RF Radio Frequency

RF-ID Radio Frequency Identification

SH Sample and Hold

TEG Thermo Electric Generators

TFF Toggle Flip Flop

TSMC Taiwan Semiconductor Manufacturing Company

VCO Voltage Controlled Oscillator

OTA Operational Transconductance Amplifier

1. Introduction

Energy harvesters are devices which can gather energy from their surroundings. Various types of energy harvesters that generate electrical energy from different energy sources are available. Energy harvesters can be used to power small loads and eliminate their dependence on batteries. Batteries run out and their replacement might not be possible especially if these systems are situated in locations or areas that are hard-to-reach. In such situations, batteries can be potentially replaced by energy harvesters [1].

Examples of such systems are wireless sensor nodes which detect natural disasters like forest fires, earthquakes, landslides and tsunamis [2]. Such monitoring sensors are designed to send alarm signals. Battery maintenance of a large-scale network, consisting of a substantial number of sensor nodes, may be difficult and costly. Energy harvesters, as a replacement for batteries minimises the maintenance and the cost of operation. Power scavenging may enable wireless and portable electronic devices to be completely self-sustainable, so that battery maintenance can be eventually eliminated [1].

Another application for such harvesters are sensors, which continuously monitor air quality in cities and sensors which monitor stresses in building structures. Such sensors send alarm signals in case abnormal levels are reached [2]. Maritime and wildlife organisations also install devices on animals for monitoring purposes and

research, and it would be advantageous if such devices are not dependent on their battery's lifetime [3].

Currently available medical devices, such as cardiac pacemakers or deep brain stimulation devices may be implanted in the body [2, 4]. Presently such implanted devices are battery operated and over a number of years, the patient has to undergo surgery for battery replacement [5].

Although energy harvesters feature a number of challenges, if properly designed can provide an adequate replacement to batteries so that the devices they power, work indefinitely. Most currently available off-grid devices and portable sensors rely on batteries to get powered. It would be much more convenient if these batteries are replaced by an energy harvesting device whenever a wired power supply via cable is not available or the maintenance expenditure to replace dead batteries is too high. Such sensors would use harvested electrical energy to power their associated microprocessor, conditioning circuitry, and communication interface.

1.1 Main Objectives and Methodology

The aims and objectives of this research were to investigate and develop a novel power conditioning circuit which is capable to work with various types and models of energy harvesting devices that feature different output characteristics. The proposed circuit targets energy harvesters having an output voltage ranging from 1 V to 40 V Alternating Current (AC) or Direct Current (DC) and an output power in the micro-watt and milli-watt range. The power conditioning circuit drives the energy harvester at a maximum power point and the output voltage is regulated to an adjustable constant output voltage as required by the load. Additionally, energy storage is possible so that any excess energy is stored for later use, to minimise the down time of the load. In order to reach this objective and obtain a reliable and efficient power conditioning circuit for various energy harvesters, several studies and

investigations on innovative designs and fabrications were carried out throughout this research. All the designed circuits were implemented in an integrated circuit in order to ensure that the designs also work as expected once they are fabricated.

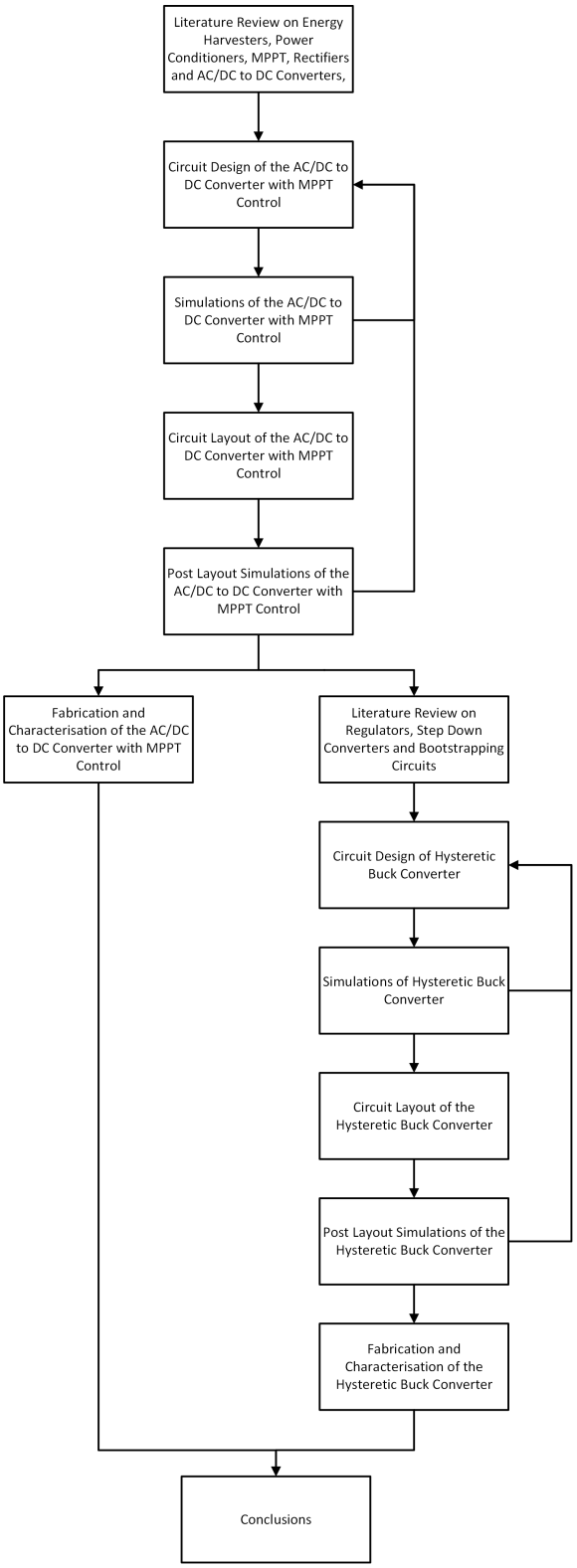

Figure 1.1: The research methodology

Figure 1.1 illustrates the research methodology employed throughout this work. A literature review on the state-of-the-art on energy harvesting techniques, power conditioning circuits, regulators, bootstrapping circuits and converter topologies has been conducted. Conclusions from this literature review were drawn to identify the research gaps and propose a novel implementation for the power conditioning circuit.

1.2 Contribution to Knowledge

Portions of the research work reported in this dissertation has been published in five peer-reviewed conference papers and a peer-reviewed journal paper.

The proposed novel architecture of the power conditioning circuit has an MPPT compatible with different energy harvesters, is capable to work with both AC and DC input voltages, has capacitive energy storage, and outputs a regulated voltage [6]. This architecture is an innovative approach from the two schemes being investigated in [7]. Single stage schemes only utilise a full wave rectification stage either using passive or active rectification whereas two stage schemes proposed in [8, 9] consist of a full wave rectification stage using either passive or active rectification, a temporary storage capacitor and a DC-DC converter to generate a regulated output voltage. Although having a separate rectifier and converter has the advantage of simplification and allows for better analyses and control of the circuitry, the operating efficiency in this project is very important because the power conditioner is designed for microwatt and milliwatt range energy harvesters. Such low power is easily wasted in switching losses, conduction losses and control circuitry. Therefore particular attention and decisions were taken at all design stages in order to choose the least complicated options with minimal energy losses.

This architecture makes use of a direct AC/DC-to-DC converter which has never been implemented inside an integrated circuit before. Improvements to the

converter topology for better efficiency and performance were also implemented. Testing of the fabricated converter resulted in a peak conversion efficiency of 63.4%. Due to the converter type, no rectification is required when connecting the proposed power conditioning circuit with energy harvesters having an AC output voltage. As a result, another novelty of the proposed power conditioning circuit is that it can work with piezoelectric, pyroelectric, photovoltaic, electromagnetic, electrostatic and thermoelectric energy harvesters and operate all energy harvester types and models at maximum power point also due to the Maximum Power Point Tracking (MPPT) algorithm adopted. The MPPT controller is capable of reaching Maximum Power Point (MPP) by only sensing the output voltage as in [10, 11] and therefore there is no need for current sensing, which is a high power dissipating block.

Testing of the fabricated circuit shows that the MPPT circuit is capable of maintaining the energy harvester operating within 99% of its maximum power point. The power consumption of the MPPT circuit is 2 µW [12]. All control circuitry is implemented in analogue electronics to obtain higher efficiency because microprocessors, Analogue to Digital Converter (ADC), Digital to Analogue Converter (DAC) and clocks consume a substantial amount of power which is sometimes higher than the power available from energy harvesters. Additionally all transistors operate in the sub-threshold region to limit the current flowing through the transistors, thus further reducing power dissipation.

The first stage of the proposed power conditioning circuit, consisting of the AC/DC-to-DC converter with MPPT function, uses two on-chip low precision, low power, and low frequency oscillators [13]. These oscillators make use of an improved design of a self-biased, temperature and supply voltage independent, current reference circuit with transistors operating in the sub-threshold region. This current reference circuit was designed specifically for the oscillators in this power conditioning circuit. Two oscillators, one generating the 15 Hz clock frequency for

the MPPT algorithm and the other generating the 200 kHz sawtooth wave required for the pulse width modulation to operate the switch mode converter, were designed in this work [12]. Both these low power oscillators are fully integrated with no external components. The results obtained during characterisation are included in this dissertation. Both the 15 Hz oscillator and the 200 kHz sawtooth generator work with a supply voltage of 1 V and have a power consumption of 30 nW and 63 nW respectively.

The second stage of the power conditioning circuit consists of three externally adjustable buck converters to supply a constant output voltage for the load and for the control circuits in the power conditioning circuit. An innovative fully integrated capacitively coupled bootstrapping circuit was implemented in this stage to drive the high side NMOS transistor of every buck converter [14]. The buck converters are controlled by a novel hysteretic control with variable power consumption depending on the output voltage quality required.

Characterisation of the fabricated circuit show that the novel circuitry implemented in this power conditioning circuit, works as predicted by the simulations [15]. The control circuitry consumes between 194 µW to 420 µW, depending on the biasing current at which it is operated. The integrated AC/DC-to-DC converter obtained a peak conversion efficiency of 84.2% [15]. The hysteretic control is able to maintain the set output voltage at all times and at all input voltages. Compromising between output ripple voltage and control circuit power dissipation is possible by varying the bias current of the comparator.

1.3 Dissertation Organisation and Summary

This dissertation is divided into six chapters, describing in detail the achievements and contributions of this PhD research. This chapter introduces the research aims and objectives, and the papers published throughout this research.

- **Chapter 2** presents a literature review including the state-of-the-art on power conditioning circuits, power converters, rectification, maximum power point tracking circuits for low powered energy harvesting, voltage regulators and step-down converters.

- **Chapter 3** discusses in detail the proposed novel power conditioning circuitry and its innovative aspects. This chapter includes a detailed documentation on the rationale behind the decisions taken during the design of the power conditioning circuit. Such decisions were also based following the research gaps identified in the state-of-the-art in Chapter 2. The discussion is also supported by similar other research studies and preliminary simulations carried out.

- **Chapter 4** presents and discusses the design of the AC/DC-to-DC Converter with MPPT Control Circuit. The discussion is aided by means of a number of simulation results, circuit layout considerations, and post-layout simulations. The experimental results of the circuit are also presented in this chapter.

- **Chapter 5** presents and discusses the design, circuit level simulation, layout considerations and post layout simulation of the fabricated voltage regulating buck converter. This chapter also presents the experimental measurements of the final fabricated circuit.

- **Chapter 6:** This chapter outlines the main contributions to knowledge attained via this research. It also proposes a potential road map to aid further research which can be carried out as a continuation to what has been obtained in this work.

2. Literature Review

Energy harvesters are devices which can convert energy available within their surroundings into useful electrical energy. There are numerous sources for energy harvesting such as solar energy captured by solar cells, temperature difference captured via thermoelectric and pyroelectric energy harvesters, electromagnetic radiation scavenged by Radio Frequency (RF) harvesters and vibrational energy captured by piezoelectric, electromagnetic, or electrostatic energy harvesters. Solar energy harvesters (solar cells) and Thermo Electric Generators (TEG) both generate a DC voltage while all the other types of energy harvesters generate an AC voltage. Hence, the initial stage of a typical power conditioner, which converts the AC voltage into a DC voltage, may be bypassed for such energy harvesters.

In this chapter a detailed overview of the available energy harvesting sources is presented. In addition, the state-of-the-art of the electrical interfaces which can be interfaced to energy harvesters is reported. This chapter also discusses, rectification circuits which are currently being used for energy harvesters producing an AC voltage, converter topologies currently being implemented to convert input voltages generated by energy harvesters, maximum power point tracking algorithms and the state-of-the-art of their implementation as an integrated circuit.

The output characteristics of energy harvesters are highly volatile, and such devices generate a voltage and power which depend on their current operating conditions.

This is unlike a battery, which supplies a stable voltage supply throughout its lifetime. Hence, the voltage generated by an energy harvester is normally neither constant nor continuous. This means that a power conditioning circuit is required to manage the harvested power and generate a constant and possibly continuous output voltage as required by the load being supplied by the energy harvester. The power conditioner should conserve any excess power being generated, so that when the energy harvester is not generating enough power, the stored energy can be utilised to allow longer operating periods by the loads. The efficiency of the power conditioner is very important since the energy generated by the energy harvesters is already very limited and any inefficiencies would further reduce this energy.

2.1 Literature on Energy Harvester Types and Applications

2.1.1 Electromagnetic Radiation Energy Harvesting

2.1.1.1 Solar Energy Harvesting

Solar Energy Harvesting consists of the conversion of solar electromagnetic energy into electrical energy. This happens due to the photoelectric effect of a p-n junction [16]. The solar energy available is around $0.1\,\mathrm{mW\,cm^{-2}}$ indoors and $100\,\mathrm{mW\,cm^{-2}}$ outdoors, however the power harvested with current technology is $10\,\mu\mathrm{W\,cm^{-2}}$ and $10\,\mathrm{mW\,cm^{-2}}$ respectively [17]. The output voltage of solar cells is DC in nature, which eliminates the need of rectification, hence losing less energy in the power conditioning circuitry. The available output voltage and output current depend on the light incident to the cell which is available only during day, in sunny periods and from light sources if situated indoors. This makes it essential to store the excess energy generated when light is available, if the load being powered is required to work with a minimal down time.

2.1.1.2 Radio Frequency Energy Harvesting

In densely populated areas, there are numerous RF sources such as radio and TV broadcasting antennas, wireless networks, mobile phone networks and Global Positioning System (GPS) navigation systems. These sources can potentially power up loads which consume low power via RF energy harvesters. An RF harvester normally collects these radio signals through a rectifying antenna or rectenna constructed with a Schottky diode which is placed between the dipoles of an antenna [18]. The power density of mobile telecommunication RF is $0.3\,\mu W\,cm^{-2}$ of which $0.1\,\mu W\,cm^{-2}$ of power can be scavenged [17]. The state-of-the-art of these harvesters is still quite novel and the power generated is so small that very few electronic devices can be powered adequately. However, future fabrications with lower power consumption and improvement in the RF energy harvesters themselves might make this technology more viable [19].

A different use of RF energy harvesters which are being implemented commercially is in Radio Frequency Identification (RF-ID) cards. When these RF-IDs are exposed to high power electromagnetic energy from an RF reader, they generate enough energy to send a signal back to the reader with its unique code. Such technology is being used in access systems and vehicle key immobilisers. Another use of RF energy harvesters are in medical monitoring, machining-condition monitoring and structural-health monitoring [20]. Sensors are powered up the same way as in RF-IDs and sensor data is sent wirelessly back to the reader.

2.1.2 Kinetic Energy Harvesting

2.1.2.1 Piezoelectric Energy Harvesting

A piezoelectric transducer is a material which when mechanically stressed generates a voltage [21]. If a cantilever is attached to such a piezoelectric transducer, a vibration energy harvester is obtained. These harvesters are able to scavenge energy

from mechanical vibrations and convert it into electrical energy [22]. The direct electrical output from the piezoelectric transducer in a vibration energy harvester is an AC signal whose frequency corresponds to frequency of vibration of the transducer which normally corresponds to its natural frequency. Hence the initial part of the power conditioning circuit required for such harvesters should consist of an AC to DC rectifier. The voltage magnitude can reach up to 20 V in medium range piezoelectric harvesters [23]. The typical amount of power harvested from a piezoelectric vibration energy harvester from industrial applications is $116\,\mu W\,cm^{-2}$ [24]. The power available in such scenarios ranges from $1\,mW\,cm^{-2}$ at a frequency of 5 Hz to $10\,mW\,cm^{-2}$ at a frequency of 1 kHz [17]. Hence there is still potential for improvement in the harvested power from vibrational energy harvesting since the harvested electrical power is less than 5% of the available vibrational power. In order to maximise the power generation, the harvesters must be excited as close to their resonant frequency as possible. The typical piezoelectric resonant frequency is higher than 100 Hz [25, 26, 27, 28, 29]. Harvesting energy from the lower frequency, such as in motions made by the human body or moving objects, which are typically less than 50 Hz, is also attractive and comes with great challenges [30]. Vibration energy available from the human body ranges from $0.5\,mW\,cm^{-2}$ at a vibrational frequency of 1 Hz to $1\,mW\,cm^{-2}$ at a vibrational frequency of 50 Hz. With the state-of-the-art power conditioning circuits, the harvested power can reach $4\,\mu W\,cm^{-2}$ [17].

2.1.2.2 Electrostatic Energy Harvesting

The electrostatic generator principle is achieved when a transducer moves against an electric field, which generates a potential difference. There are two ways how to harvest energy using this technique, either by a voltage-constrained cycle or by a charge-constrained cycle. The charge-constrained cycle concept is obtained when a variable capacitor is pre-charged with a small starting voltage when its

capacitance is highest meaning when the capacitor plates are closer together. Once the transducer experiences acceleration, it moves away from the fixed plate, and this reduces the capacitor's capacitance. Since the charge remains constant, reducing the capacitance leads to a higher voltage difference between the plates which can reach a few hundreds of volts under typical operating conditions [31]. The capacitor is then discharged to 0 V to harvest the energy generated.

The voltage constrained cycle concept starts with the capacitor charged to a maximum voltage at maximum capacitance, when the capacitor plates are closest together. Then discharging takes place simultaneously as the capacitance is lowered maintaining the voltage constant. Once the minimum capacitance of the capacitor is achieved, the discharging keeps on until the capacitor voltage reaches 0 V. Although this is more complicated, the net energy gained is usually higher in the voltage-constrained cycle than in the charge-constrained cycle [32].

The proper switching of switches when charges are transferred is critical to obtain adequate efficiency of the electrostatic energy harvester. The voltage achieved will then be required to be stepped down to the required voltage levels.

2.1.2.3 Magnetic Induction Generator

A magnetic induction transducer is based on Faraday's law in which a variation in magnetic flux causes an electric field through an electrical circuit. This electric field can be achieved by flux variation either by having a moving magnet in a fixed coil or with a fixed magnet in a moving coil. The former is preferred because no flexible electrical connections are required to allow movement in the coil and hence no energy is lost due to frictional forces. The length of the coil is inversely proportional to the electric field generated and the power generated in the transducer. On the other hand, large area coils perform better than smaller transducers [33].

Two such examples of this principle in literature were found:

A 1 cm^3 electromagnetic micro-generator generated a power of 10 $\mu W\,cm^{-2}$ at a voltage of 2 V with an excitation input frequency of 64 Hz and a vibration amplitude of 1000 µm [34].

A 1 mm^3 electromagnetic micro-generator generated a power of 0.3 µW with an excitation input frequency of 4 MHz [35].

2.1.3 Thermal Energy Harvesting

2.1.3.1 Thermoelectric Energy Harvesting

Thermal energy harvesters convert any change in thermal energy to electrical energy. Thermal energy can be generated from different sources available in the environment such as persons, animals, machines, and natural sources. TEG generate electrical energy using the Seebeck effect, in which the temperature difference of a thermocouple generates an Electromotive Force (EMF). The thermocouple comprises of two dissimilar materials; a p-type and an n-type semiconductor connected in series electrically and in parallel thermally [36]. The thermal power available from heat generated by a human body can reach 20 $mW\,cm^{-2}$ whereas the thermal power available from heat generated in industrial applications is 100 $mW\,cm^{-2}$. The electrical power made available through power conditioning circuits is 30 $\mu W\,cm^{-2}$ and 10 $mW\,cm^{-2}$ respectively [17]. As in solar energy harvesting, the output voltage of TEGs is a DC voltage. This makes the power conditioner design simpler since rectification is not required.

2.1.3.2 Pyroelectric Energy Harvesting

A pyroelectric capacitor generates a voltage whenever it experiences a temperature change. A Micro-Electro-Mechanical System (MEMS) pyroelectric generator consists of a pyroelectric capacitor placed on a bi-metal cantilever to oscillate between a hot and a cold surface. When the pyroelectric capacitor at the tip

of the cold cantilever meets the hot surface, it heats up and moves back to the cold surface until it loses the heat again. These oscillations generate an AC voltage [22]. The area of a typical MEMS pyroelectric generator is $1\,\mathrm{mm}^2$ making it useful to place thousands of them on a substrate to obtain higher power ratings. Although this technique is still quite new, the results reported are quite promising. The typical amount of power density harvested from MEMS pyroelectric generators can reach around $1\,\mathrm{W\,cm}^{-2}$ [37]. Pyroelectric generators are quite novel technology and therefore, power conditioning circuits specifically designed to work with pyroelectric generators do not currently exist. However, the power conditioner required for both piezoelectric and pyroelectric generators are fundamentally the same, since both harvesters generate an AC voltage with approximately the same magnitude and frequency.

2.2 State of the Art of Power Conditioning Circuits for Energy Harvesters

There are two common methods used by energy harvesting electrical interfaces. One method is to directly feed the amount of power required by the load, from the energy harvester. This method either assumes that the energy harvester will be generating enough power at all times, or it is acceptable that the load would periodically stop operating due to a lack of power being generated. The second method uses a converter to harvest the maximum power available from the energy harvester and store it in a storage element. This method is more efficient and reduces the down time of the load since energy from the energy storage can be used when the energy harvester is generating less power than that required by the load. The storage element, mainly a high storage capacitor or a rechargeable battery is charged during periods of excess generated power so that the periods during which the supplied power to the load is interrupted is kept to a minimum. Since

the power and the voltage generated by an energy harvester are highly variable, because they are dependent on the power available to the energy harvester, both methods require voltage regulation so as to generate a constant output voltage to match the load requirements.

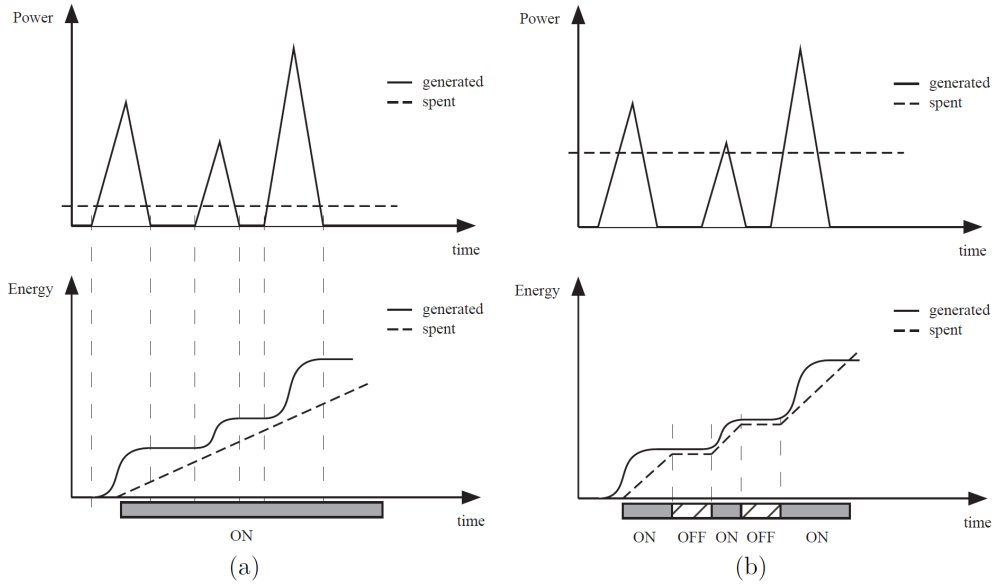

Figure 2.1: Continuous operation (a) and Discontinuous operation (b) of an energy harvester supplying a load with a constant power operating at variable operating conditions backed with a storage element [19].

When the average power consumption of the load being powered is lower than the average power being generated by the energy harvester as shown in Figure 2.1(a), then the system manages to operate continuously. During such operation, excess power is stored in the storage element so that the energy stored is used to compensate during periods of low power. On the other hand, when the average power consumption of the load being powered is higher than the average power being generated by the harvester as shown in Figure 2.1(b), then the system is

unable to operate continuously. The design of the energy harvesters and their respective conditioning circuitry is critical to get minimum interruptions of power. First and foremost, the sensors and circuitry being powered from energy harvesting need to operate as efficiently as possible with minimal dissipation of energy so that the power demand is kept to a minimum. Secondly, the circuit and components of the charge conditioning circuitry must be designed and optimised to operate with minimal self-power consumption during operation. The type of energy harvester is also critical and should be decided depending on the location where it will be operating and what environmental energy is most reliable, constant, and sufficient. The size of the energy harvester is directly proportional to the power output of the harvester. However, in certain applications such as in the medicine domain, size is a crucial component especially in implanted devices and a compromise between power generation and size has to be reached.

2.2.1 Rectification Stage

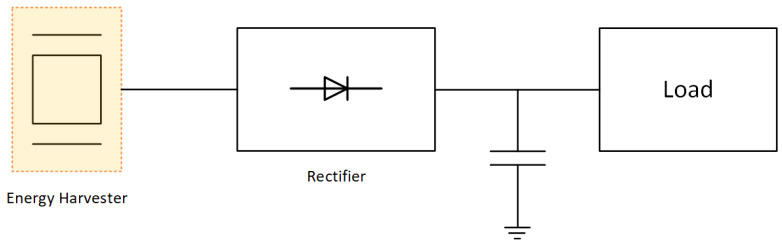

Figure 2.2: Single stage scheme [7]

Various energy harvesters such as RF harvesters, piezoelectric harvesters, magnetic induction generators, and pyroelectric harvesters generate an AC output voltage. There is an ongoing research in which asynchronous electronics are designed to operate on an alternating supply to avoid the requirement of rectification and save the power lost during this process [38, 39]. Asynchronous topologies are clockless and rely on event driven switching. Such topologies work efficiently on an AC supply. However, since this idea is still primitive, most power conditioning circuits

either use a separate rectification stage as an initial stage to convert their input AC voltage to DC voltage or the single stage scheme as shown in Figure 2.2 [7]. The single stage scheme uses just a rectification stage between the energy harvester and the load. There are several ways to implement rectification. These are further discussed below.

2.2.1.1 Passive Rectification

The simplest way and most used circuit to achieve rectification is the passive full wave rectifier circuit which consists of four diodes. The main contributor to the power loss in full wave rectification is the voltage drop of the diodes during forward biased operation. The total voltage drop across a diode is the sum of the voltage required to forward bias the diode and the conduction loss directly proportional to the on resistance of the diode. The typical voltage drop of diodes is between 0.5 V and 0.7 V. Another loss experienced by diodes is the leakage current when the diodes are reverse biased. In order to minimise the losses incurred by diodes, Schottky diodes are sometimes used which are able to operate with a lower voltage drop typically around 0.2 V but at the expense of higher leakage currents and more expensive fabrication costs since they are not directly compatible with CMOS fabrication processes [40].

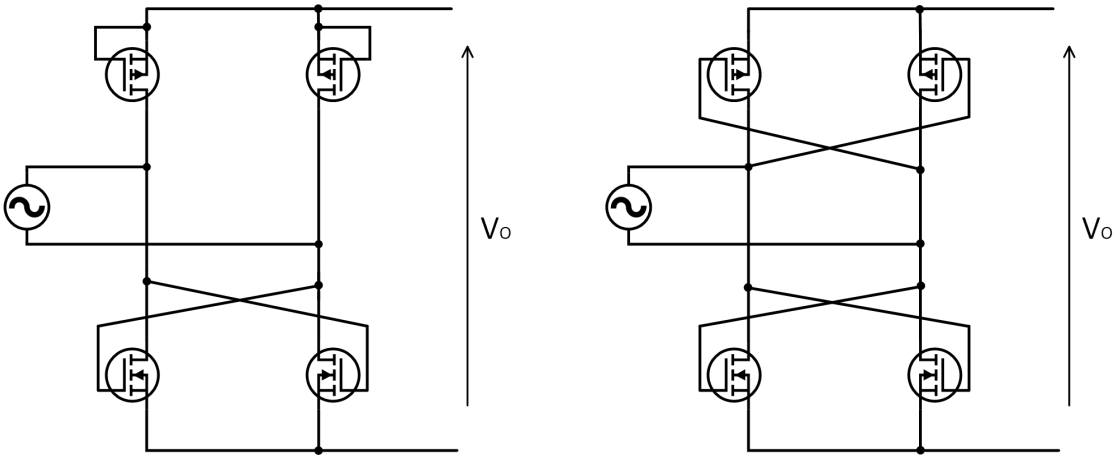

Figure 2.3: Gate Cross-Coupled NMOS and Diode-Connected PMOS Rectifier, Gate Cross-Coupled NMOS and PMOS Rectifier [41]

Several other topologies which further reduce the voltage drop across the diodes exist. Two such topologies are shown in Figure 2.3. The first topology presents a gate cross-coupled NMOS and diode-connected PMOS rectifier circuit while the second topology presents a gate cross-coupled NMOS and PMOS rectifier circuit [42]. Cross-coupled transistors in rectifiers can reduce the voltage drop to 0.1 V. However, the limitation of such circuit is that an input voltage higher than 1 V is required in order to completely switch on and off the MOSFETs [42]. Higher dissipation is experienced at voltages lower than 1 V. The turn-on threshold voltage (forward voltage) of diode-connected transistors can be further reduced by employing either pre-charged floating gate transistors, biasing of transistors at specific voltage levels or bootstrapping circuitry. In order to minimise the losses and simplify the design in integrated circuits, diodes are sometimes implemented via diode-connected MOSFETs in which the gate and source are tied together to achieve a two terminal component [43, 44]. The performance of such diodes is dependent on the threshold voltage of the MOSFETs of that particular fabrication technology and also the circuit design and sizing. Lower threshold voltage transistors are sometimes offered in advanced CMOS technologies, however at an extra cost because additional fabrication steps would be required [45]. Another

option is the threshold voltage cancellation technique by employing biasing circuits, although this approach does not allow the transistors to completely turn on and off. This leads to an increased voltage drop across the diodes and an increase in leakage currents may also be experienced [45].

2.2.1.2 Active Rectification

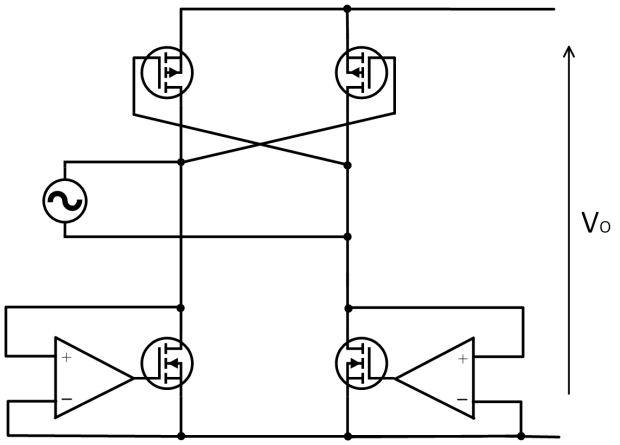

Figure 2.4: Gate Cross-Coupled PMOS and Active NMOS Rectifier [41]

Active rectifiers replace diodes with comparator-driven MOSFETs. The comparator continuously measures the voltage difference between the drain and source of the MOSFET and is optimised to switch on and off the MOSFET at the most effective timing. Consideration needs to be taken during the zero crossing so that no power is lost due to switching delays and to avoid periods in which all transistors are switched on simultaneously thus shorting the input. Usually comparators having a high slew-rate are used so that turn-on and off delays are kept to a minimum. However, high slew rate comparators require high biasing currents which dissipate more power [46]. Therefore a compromise between power dissipation and delays has to be found [43]. Active rectification improves the power dissipation in diodes but additional power dissipation is introduced in the comparators [47]. Nonetheless if designed correctly, active rectifiers can still obtain higher conversion efficiency than passive rectifiers. Some reported power

consumption values achieved by active rectifiers are 50 nA at an rms input voltage of 3.3 V which is equivalent to 165 nW [48] and 3.3 µA at 2.75 V peak to peak voltage which equates to 6.4 µW [47]. Power conversion efficiency achieved from practical results obtained from the topology shown in Figure 2.4 are between 80% and 85% at a power ranging from 10 mW to 20 mW [49] and which can reach 95% at low load conditions of 1 mA at a voltage of 2 V [50]. Another active rectifier reaches a power conversion efficiency ranging between 80% and 90% at a power of 20 µW [48]. Active rectifiers normally offer higher efficiency levels than passive rectifiers except at low power levels in which low-voltage threshold MOSFETs can achieve better efficiency mainly because active rectifiers have a base load incurred by the comparators [51].

2.2.1.3 AC to DC Direct Switch Mode Converters

AC to DC direct converters transform an AC voltage into a DC voltage without requiring a preceding rectification stage. Having a single stage converter rather than a two-stage converter (rectification stage and converter stage), is advantageous especially in low power, low voltage applications. The efficiencies of a full wave rectifier circuit alone and a two-stage energy harvesting circuit were derived, investigated and compared in [7]. However, this work does not investigate single stage direct AC to DC switch mode converters in the comparison. The single stage full wave rectifier scheme has a higher harvested efficiency if the optimal energy storage device voltage is chosen as compared with the two-stage scheme [7]. Both schemes have losses in the full wave rectifier while the two-stage approach also incurs losses in the switch mode converter. When comparing the single stage direct AC to DC switch mode converter to a two-stage converter, the single stage approach eliminates the power losses incurred in the initial rectification stage which were discussed in Sections 2.2.1.1 and 2.2.1.2. Another advantage in single stage converters when comparing them to those using a two-stage scheme

with active rectification, is having less switching devices and less control circuits. When comparing the single stage direct AC to DC switch mode converter to just a single stage full wave rectifier, the losses of rectification are replaced with the losses of a switch mode converter. An advantage of using a switch mode converter is that it can be controlled so that the energy harvester is operated at maximum power point which has the potential to harvest substantially more energy from the same harvester. There are several topologies which can achieve direct AC to DC voltage conversions which will be analysed in detail further on. Another method to maximise efficiency in low power applications is for the converters to operate in Discontinuous Conduction Mode (DCM). In DCM, all the inductor energy is utilised at every clock cycle and so the current flowing in the converter upon switching is zero. Thus, the switching devices switch off at zero current and hence a converter operating in DCM reduces the switching losses in all diodes and transistors and reverse recovery losses in diodes [31]. Also converters operating in DCM require smaller passive devices than when operating in Continuous Conduction Mode (CCM).

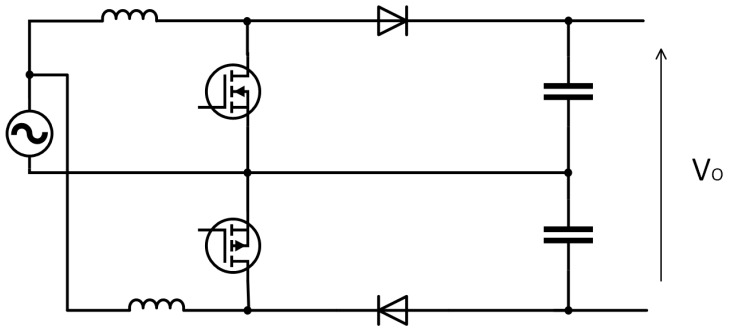

Figure 2.5: Dual Polarity Boost Converter [31]

A dual polarity boost converter shown in Figure 2.5, consisting of essentially two boost converters, one for the positive half cycle and another for the negative half cycle was proposed in [31]. The operation of the boost converters alternates depending on the polarity of the input cycle. The components required are two

switching devices, two diodes, two inductors and two capacitors. An issue with this standard dual boost version is that it can only work when the maximum input voltage is less than the threshold forward voltage of the parasitic diodes in the MOSFETs. In a practical test, a power conversion efficiency of 44% was recorded with an input power of 49 mW [31]. An improvement to this topology is the secondary side switch based direct AC to DC single inductor converter shown in Figure 2.6 (a) [52]. This topology makes use of a single inductor, two diodes, a single capacitor and four switching devices. Two of the switching devices are a PMOS and an NMOS transistors which create a bidirectional boost switch. These switches are switched on and off simultaneously and irrespective of the input voltage polarity. The secondary side switches are switched on and off according to the polarity and with the same frequency of the input voltage. Hence polarity sensing is necessary for this topology.

The split capacitor direct AC to DC single inductor converter is shown in Figure 2.6 (b) [52]. This topology is made up of a single inductor, two diodes, three capacitors and two switching devices. A PMOS and an NMOS transistors are used to create a bidirectional boost switch. The low number of components makes this topology one of the simplest and most efficient. Another advantage of this topology is that there is no need to sense the polarity of the input voltage to control the converter accordingly. Considering the low power levels available from energy harvesters, this is beneficial since less power is lost in the control circuitry. A disadvantage of the split-capacitor version is that each of the split capacitors is charged only for one half cycle of the energy harvester's frequency. Therefore, large voltage ripples are experienced in the converter's output. Hence to maintain the voltage ripple within an acceptable limit, an extra output capacitor is sometimes used, which in most cases is impractical due to the size restrictions of the power conditioning circuit. Moreover, a large output capacitor slows the converter's response [52].

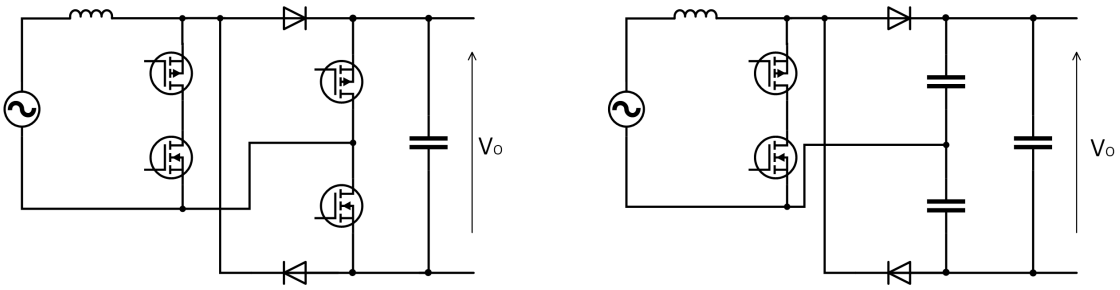

Figure 2.6: AC to DC Single Inductor Direct Converter Topologies (a); Secondary side switch-based version and Split-capacitor version (b) [52]

The Dual Polarity Boost converter was improved so that only one capacitor and one inductor are required as shown in Figure 2.7. In some cases, the inductance required can be obtained by the parasitic inductance of the energy harvester. Although this improved topology can work with voltages higher than the threshold forward voltage of the parasitic diodes in the MOSFETs , the current required to charge the inductor during the on state, must go through the parasitic diode in the switching device of the non-operational boost converter to complete the loop. This incurs an additional voltage drop which results in additional power loss. In a practical test using discrete components, a power conversion efficiency of 80% was recorded with an input power of 100 µW, however when including the losses in the ancillary circuits this efficiency drops to 44% [53].

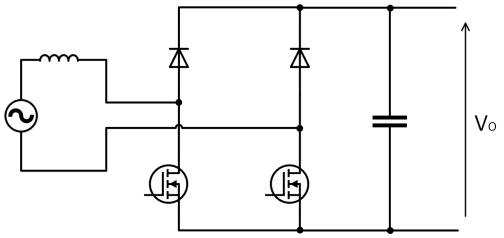

Figure 2.7: Dual-Boost AC to DC Direct Converter Improved Version [53]

A combined Boost and Buck-Boost AC to DC Direct converter is shown in Figure 2.8 [54]. The Boost converter operates during the positive half cycle whilst the Buck-Boost converter operates during the negative half cycle. The components

required for this topology, are two inductors, two switching devices, two diodes and a capacitor. This AC-DC converter has the same issue of the original dual boost AC-DC converter version whereas this dual boost topology can only work when the maximum source voltage is less than the threshold forward voltage of the parasitic diodes in the MOSFETs . A major disadvantage of this converter is that the converters are different and hence a fully independent control system is required for them to operate. The efficiency recorded during experimental results of this topology when implemented using discrete components was of 63.8% with a source voltage amplitude of 400mV, frequency of 100Hz and a power of 100 mW [54].

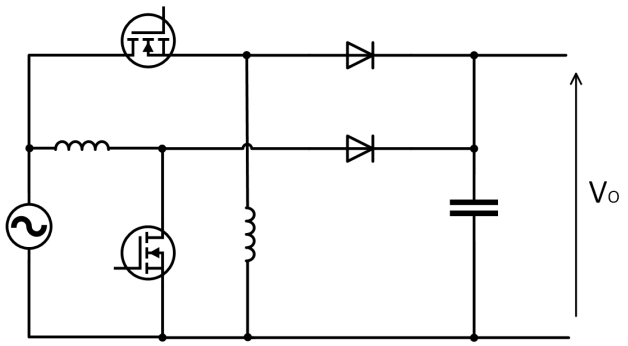

Figure 2.8: Combined Boost and Buck-Boost AC to DC Direct Converter [41]

2.3 MPPT in Nanoscale Electronics

All energy harvesting devices can supply their maximum power when they are being operated under ideal load conditions. The maximum power is extracted from the harvester when the impedance of the load matches the impedance (internal resistance) of the energy harvester. The internal resistance of an energy harvester is not constant and varies with the current operating conditions which depends on the ambient conditions and power available. In order to continuously match the load resistance, there are numerous Maximum Power Point Tracking (MPPT) techniques which continuously scan for and apply the load condition at which the

harvester supplies the maximum power available. Impedance matching is most achieved by varying the operation of the DC-DC converter via duty cycle control in order to adapt to the changes in the ambient conditions and the load conditions of the energy harvester since its output is not regulated to a fixed voltage or power level. The MPPT should be able to prevent voltage collapse, which is a runaway condition that occurs when the loading power is higher than the power available from the energy harvester, thus draining higher current as the voltage and power levels keep collapsing towards zero [55]. Most commonly known switch mode DC-DC converters are capable of obtaining the MPPT function by controlling the duty cycle of the switching device or devices. Obtaining the MPPT function in switched capacitor converters is much more challenging although this is still possible [56].

2.3.1 Maximum Power Point Tracking Techniques

There are four main maximum power point tracking algorithms reported in literature: Fractional Open Circuit Voltage, Fractional Short Circuit Current, Perturbation and Observation (PO) and Incremental Conductance.

2.3.1.1 Fractional Open Circuit Voltage Algorithm

This algorithm is mostly used for solar energy harvesters. The maximum power point voltage of a solar cell or cells is linearly proportional to the open circuit voltage under all ambient conditions [57]. Hence, the MPPT periodically disconnects the load and measures the open circuit voltage of the solar cell. The MPPT then operates the harvester at the calculated voltage once it is multiplied with a predetermined constant. This constant varies with the type of solar cell, which makes it essential that the MPPT is either specifically designed for a particular type of cell or needs to be preset with the constant corresponding to the type of cell being used. Another disadvantage of this technique is that every

time the MPPT measures the open circuit voltage, there is a period in which no power is being generated. The time of disconnection should be as short as possible to minimise the energy loss but long enough to allow the voltage to settle before taking the open circuit voltage measurement. This method is simple and robust but the constant may vary over time due to deterioration of the energy harvester which may end up operating the harvester at a voltage in which maximum power is not being extracted [58]. Although this algorithm is mainly used for solar energy harvesters, it may also be used for other types of harvesters given that there is linear dependency between the maximum power point voltage and the open circuit voltage under all ambient conditions and the operating conditions of the energy harvester.

2.3.1.2 Fractional Short Circuit Current Algorithm

This algorithm is also mostly used for solar cell applications. The maximum power point current of a solar cell is linearly proportional to the short circuit current under all ambient conditions [59]. Similarly to the previous algorithm, the MPPT periodically short circuits the harvester and measures the short circuit current of the energy harvester. Then the MPPT operates the harvester at the current calculated by multiplying a constant value with the short circuit current. Same as in the previous algorithm, the MPPT must be specifically designed or preset for the harvester which it will be connected to. Determining the short circuit current is even more challenging because an additional transistor and a current sensor are required. It is important for the heat dissipation to be catered for and ensure that the transistor shorting the energy harvester's output has an adequate current capability. Another disadvantage is that current measurement is more challenging than voltage measurement [58]. This algorithm also has the same disadvantage that during the short circuit current measurement, there is no power being generated. This algorithm may only be implemented to other types of harvesters if there is

linear dependency between the maximum power point current and the short circuit current under all operating conditions and ambient conditions of the harvester.

2.3.1.3 Perturbation and Observation (PO) MPPT Algorithm

The Perturb and Observe (PO) is the most popular MPPT algorithm due to its simplicity and efficacy. Several variants of the PO algorithm were developed throughout the years, but the basic technique is to periodically sense the voltage and the current being harvested, multiply them to obtain the power and store the data. Then the operating voltage at which the harvester is being maintained by the converter via its duty cycle is perturbed in a given direction either higher or lower. Then the voltage and current is measured again to compare the power at the new voltage level. If the power is higher, then the operating voltage is perturbed again in the same direction. If not, the operating voltage is varied in the opposite direction. Numerous ways exist how to obtain the following algorithm especially in analogue integrated circuits. The comparison of the power at the previous operating voltage to the power at the current operating voltage can be obtained either by a differentiator operational amplifier circuit or a comparator. The voltage, current or power levels at the original operating voltage level can all be stored in sample and hold operational amplifier circuits. The disadvantage of such algorithm is that during steady state, the power level oscillates around the optimum power which results in a slight loss of power. For this reason, such MPPT circuits usually quote the percentage efficiency of the MPPT. The advantage of this algorithm is that it is compatible with various types of energy harvesters and if the energy harvester is changed, MPPT is still obtained without the need of any modifications to the control circuitry [16].

2.3.1.4 Incremental Conductance Algorithm

The Incremental Conductance algorithm depends on the fact that the slope of power curve versus voltage $\left(\frac{\delta P}{\delta V}\right)$ is zero at maximum power point, positive on the left side and negative on the right side. For MPPT operation, the voltage derivative, current derivative, and power derivative are measured and calculated [58]. This algorithm compares the incremental conductance $\left(\frac{\delta I}{\delta V}\right)$ to the instantaneous conductance $\left(\frac{I}{V}\right)$. MPP occurs when $\frac{\delta I}{\delta V} = -\frac{I}{V}$. If this equation is not satisfied, the operating voltage of the harvester is then increased or decreased depending on the result [60]. This algorithm is also compatible with various types of energy harvesters. The advantage of the Incremental Conductance algorithm is that once the maximum power point is determined, unless there is a change in current, MPP tracking is stopped, thus maximising efficiency unlike in the Perturbation and Observation algorithm. However, this algorithm is more complex than the PO and is usually implemented using a multiprocessor since implementing it in integrated analogue electronics is challenging.

2.3.2 State of the Art of Maximum Power Point Tracking Circuits

A Maximum Power Point Tracking circuit device developed for vibration energy scavenging in micro-power applications was published in [61]. This circuit uses the AMS CMOS 0.35 µm integrated circuit fabrication technology. The initial part of the circuit consists of a full wave rectifier using a hybrid rectifier shown in Figure 2.9 which is capable to self-start. The hybrid rectifier operates as a passive rectifier at voltages lower than 1.8 V while active diodes kick in at voltages higher than 1.8 V once the circuit starts up. The threshold voltage of MOS transistors in this technology is relatively high. The active diodes increase the output voltage of the rectifier by 0.5 V when compared to the passive rectifier. The maximum

input voltage of the circuit is 6 V. The harvested power reached 254 µW and the maximum efficiency excluding the rectifier's losses but including the MPPT system power loss was 95.6%. This circuit does not include a converter but generates a control voltage output so either it controls an externally connected converter to operate the harvester at maximum power point or switch on and off the load to work in burst mode [61].

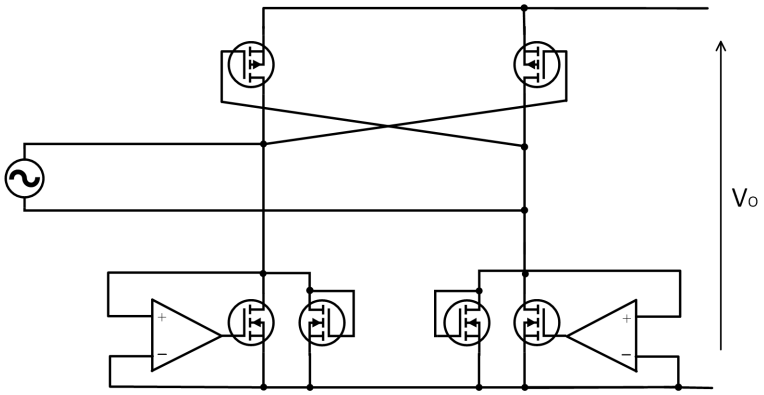

Figure 2.9: Hybrid Rectifier as proposed in [61]

A self-biased fully analogue MPPT circuit designed for piezoelectric or electrostatic energy harvesters in [62, 63], has an input voltage range of 5 V to 60 V with an input power ranging from 25 µW to 1.6 mW. This power conditioning circuit was implemented using the TSMC 0.25 µm Bipolar CMOS DMOS (BCD) process technology with the 60 V option. The output voltage can range from 2 V to 5 V. The converter efficiency excluding the full wave rectifier reaches 88.9% at an input voltage of 30 V. This circuit requires an externally connected load battery to store the harvested energy. The MPPT algorithm implemented is the Perturbation and Observation method with variable step function. This means that the step size is larger when it senses that the power being harvested is far from the optimum level. The MPPT efficiency reached 99.9% and its respective operating current ranged between 900 nA to 1.3 µA which equates to a scavenging power of 5 µW. An on-chip Buck DC-DC converter was implemented as part of this circuit. However,

the rectifier is not included and has to be externally connected together with an inductor, a load capacitor and a battery [62, 63]. Since the converter topology employed is a Buck converter, this MPPT conditioning circuit is only capable to step-down the input voltage.

The same authors improved the first design by including the cold start-up feature and also the circuit was modified so that it does not require an external battery but two externally connected input and output capacitors. The output voltage range of the improved version is from 0 V to 5 V. The input power ranges from 1 µW to 1 mW. A lower control power loss of 500 nW was also achieved. However, the converter efficiency still dropped to 85% excluding the full wave rectifier loss since this has to be connected externally. The circuit control is powered via the output of the converter since this circuit can operate with an input voltage up to 60 V. The cold start-up of the circuit operates by shorting the input side to the output side, so that the load capacitance is charged. Once the voltage across the load capacitance reaches a programmable threshold voltage, the control circuit fires up. The circuit requires one inductor, two capacitors and two resistors to be connected externally apart from the full wave rectifier which is not implemented as part of the integrated circuit [64].

Another Maximum Power Point Tracking circuit is designed for Piezoelectric energy harvesting in [65]. A Buck-Boost converter uses the 0.35 µm BCD process technology. The input voltage range of the circuit is from 1 V to 7 V and the output voltage can range between 1 V and 8 V. The MPPT algorithm implemented is the fractional open circuit voltage. This is achieved by a peak detector and a switching controller which periodically opens the circuit so that the peak detector samples the open circuit voltage. A small sized sensing capacitor is used by the peak detector so that it can sample the open circuit voltage in just one cycle. This MPPT operates the energy harvester at half the open circuit voltage. The maximum converter efficiency achieved, excluding the rectifier losses is 80%. The open circuit voltage

sensing time is just one cycle and the MPPT tracking takes 20 ms when the input MPP voltage changes from 3.4 V to 1.2 V, which equates to a tracking time of 9.09 ms V^{-1}. The MPPT efficiency reaches 99.9%.

An efficient solar energy harvester, designed for wireless sensor nodes in [66], uses the constant voltage tracking maximum power point tracking algorithm. The circuitry is implemented using discrete components with a 400 mW poly-crystalline solar panel. The overall efficiency of the converter in this circuit is 93% and the output power ranges from 5 mW to 400 mW. MPPT is achieved by controlling a Buck converter and its output energy is stored into a capacitor. Then a Boost converter boosts the voltage to 3 V to charge the battery. The power consumption of the control circuit is 300 µW. The issue with this implementation is that the MPPT is designed to maintain the solar panel at 1.8V because it is the voltage at which this solar cell generates maximum power irrespective of the light conditions hitting the solar cell. This means that the design is only suited for this solar cell and assuming that the maximum power point voltage of the cell will remain constant at all operating conditions and throughout the lifetime of the cell [66].

A single power management circuit was designed to condition the power harvested from a hybrid indoor ambient light energy harvester and thermal energy harvester in [67]. An average electrical power of 620 µW is harvested at an indoor lux level of 1010 lux and a temperature difference of 10 Kelvin. The conditioning circuit is implemented using discreet components and off the shelf Integrated Circuits to generate the pulse width modulation (PWM) for the converters. A boost converter is designed to achieve an MPPT function. The harvested energy is stored in a super capacitor having a capacitance of 0.1 F and a maximum voltage of 5.5 V. The MPP function is achieved by a microcontroller which is set to maintain a constant voltage across the energy harvesters. A final proportional integral (PI) controller is implemented in the microcontroller to generate the PWM and achieve the set voltage. A buck converter is implemented to generate a regulated output

voltage from the storage capacitor to a lower voltage of 2.8 V. The efficiency of the MPPT Boost Converter ranges from 80% to 94%. The power consumption of the electronic circuits measures 135 µW. A disadvantage of the MPPT implemented in this publication is that a single MPPT was used for both energy harvesters which are connected in parallel via a diode. This may decrease the harvested power as both harvesters have to be operated at the same voltage. Moreover, the MPPT is preset to work with these particular harvesters thus it may not operate as expected on different types of energy harvesters [67].

A Piezoelectric energy harvesting system together with its conditioning circuitry having also an MPPT function is implemented using discrete electronic components in [68]. The MPPT algorithm adopted is the PO and this is microprocessor controlled. The DC-DC converter chosen for this application is the Flyback converter which is operated in Discontinuous Conduction Mode (DCM). Experimental results of this design harvested a power of 8.4 mW at an acceleration level of 0.5 G. The maximum efficiency reached was measured at 72% when the four parallel connected piezoelectric cantilevers vibrate at their resonant frequency of 47 Hz. The MPPT function uses the hill climbing algorithm or the Perturbation and Observation algorithm. The MPPT function is carried out using an off the shelf low power consumption microcontroller. The efficiency of the flyback converter ranges from 65% to 76%. Most of the power consumed is in the full wave rectification block. The disadvantage of this prototype is that it is quite bulky, and the power obtained is very low when compared to its size [68].

Another publication describes the design and simulation results of an integrated single output sensor maximum power point tracking circuit for Photovoltaic (PV) solar systems [69]. The technology used for this MPPT is the 0.35 µm CMOS technology. This design does not include any DC-DC converter. The circuit designed requires the voltage and current of the solar cell as input and it outputs a PWM signal to be fed to an external converter's switching transistors. The circuit

makes use of sample and hold blocks to compare the power harvested from the solar cell when it follows the PO algorithm [69].

An energy efficient power management circuit for solar energy harvesters was designed and implemented using 0.35 µm BCDMOS process technology [70]. The MPPT algorithm chosen for this circuit is the Perturbation and Observation. The system consists of an 800 µW solar cell, a Buck DC-DC converter, an MPPT block, a clock generator, and an energy storage. The solar cell used has an open circuit voltage of 5 V and a short circuit current of 30 mA. The buck converter's inductor and an energy storage device being either a battery or a capacitor are required to be connected externally. The voltage and current sensing circuits in the MPPT block are achieved by means of switched capacitor integrator circuits. Then the voltage and current are multiplied using the Gilbert cell multiplier and the current power and the previous power are compared using a Sample and Hold (SH) circuit and a comparator. The MPPT adopted a Successive Approximation Register (SAR) so that the time required for the harvester to reach maximum power point is reduced considerably. The input voltage range of the circuit is 1.5 V to 5 V whereas the output voltage could range from 0 V to 4 V. The supply voltage of the control circuitry is 3 V. This paper reports that the MPP tracking efficiency obtained with SAR was 99% compared to 97.1% in conventional MPPT. The MPPT circuit consumes a power of 4.6 µW [70].

The design and simulations of a battery less Power Management Unit (PMU) harvesting vibrational energy from a piezoelectric harvester to be used for wireless sensor nodes is proposed in [71]. The PMU rectifies the input voltage using an AC-DC doubler circuit. Then it makes use of three charge pumps with a regulated output using Low Dropout Regulator (LDR). The charge pumps power separate loads and they are switched on according to the available power or once enough energy is stored in their storage capacitor. When the harvested power is lower than the baseband power, it operates the critical loads on duty-cycled operation

while low priority loads are on sleep mode. If the harvested power is higher than the baseband power, then critical loads are operated continuously and low priority loads are operated on duty-cycled operation. If the harvested power is higher, then all loads are operated continuously. The MPPT technique used is the load perturbation technique. The system keeps trying to operate all blocks continuously starting from the high priority block and then senses the harvester's voltage. This design is very load specific, and a new design is required if this circuit is to be implemented for different loads. In order to obtain successful results from such designs, the loads have to be very flexible in terms of input power and operation in order for the MPPT to be achieved by switching on and off parts of the load [71].

An MPPT circuit for thermoelectric energy harvesters was designed in [72]. The MPPT circuit proposed was implemented using discrete analogue components. The thermoelectric generator's internal impedance was measured to be 35 Ω for all temperature gradients of the TEGs used. The DC-DC converter chosen for this circuit is the buck boost converter and is operated in DCM. For a buck boost converter operated in DCM, the impedance of the load could be controlled just by adjusting the duty cycle and the on period. The converter then charges a rechargeable battery. The problem with this approach is that the circuit must be retuned if the harvester is changed and it can only obtain maximum power point if the internal impedance of the harvester is constant throughout all its operating conditions. However, this simplistic approach made the PMU very efficient. The overall efficiency reached 85%. [72]

Another publication of a maximum power point tracking charge pump for indoor solar energy harvesting was investigated in [73]. The input voltage range of this circuit is from 1 V to 2.7 V and the output voltage is regulated by means of a low dropout regulator. The power output of this circuit can reach 80 µW and the controller power loss ranges from 450 nW to 850 nW. This circuit is implemented using the 0.35 µm CMOS technology. This energy management circuit calculates

the optimum V_{S_REF} from the Optimum Power Point Tracking (OPPT) block. Then if the feedback input voltage from the solar cell is higher than the optimum voltage, and the output voltage is lower than required, the charge pump is switched on to discharge C_{IN} to a voltage closer to the optimum voltage so that a higher power is obtained from the solar cell. The maximum efficiency of the energy management circuit is measured to be 86% at 35 µW. The disadvantage of this circuit is that there are no capacitors to store energy when excess power is being generated from the solar cell. Furthermore, the use of low drop out regulators rather than DC-DC converters may lower the efficiency of this circuit. The advantage of this circuit is that it does not use a current sensor thus reducing the power consumption [73].

A publication of a 400 nW single-inductor dual-input-tri-output DC-DC Buck-Boost converter with MPPT for indoor photovoltaic energy harvesting was analysed. The settable output voltages possible are 1 V, 1.8 V and 3 V. This circuit makes use of a battery as an energy storage. This circuit is implemented using the 0.18 µm CMOS technology. The MPPT algorithm implemented was the perturb and observe. This algorithm is activated every 3.3 seconds. The output power can range from 1 µW to 10 mW whilst the power consumption of the circuit is 400 nW. Since the output power range covers four orders of magnitude, it was essential for the clock frequency switching the MOSFETs to be varied depending on the operating power. The maximum efficiency reached 83% with the MPPT in operation [74].

Another study is a design of a micro power management system for applications using photovoltaic cells with the Maximum Output Power Control [75]. An inductorless on-chip power management system using the 0.35 µm CMOS technology is proposed. Instead of a switching DC-DC converter, this design opted for a step-up charge pump which could either power a circuit directly or use a rechargeable battery as an energy storage. The Perturb and Observe maximum

power point tracking algorithm is used in this circuit. The charge pump switching frequency varies depending on the power being harvested to minimise the system power loss. The variable switching frequency is generated via a Voltage Controlled Oscillator (VCO). The MPPT is achieved by varying the clock frequency of the charge pump after sensing the output current. Experimental results concluded that this circuit reaches a maximum efficiency of 67% and the maximum output power achieved reached 776 µW. This circuit can only operate with a DC input voltage. To connect an energy harvester generating an AC output voltage, an external rectifier is required. [75]

An energy management integrated circuit for photovoltaic cells having a minimum input voltage of 0.21 V was implemented using the 0.18 µm 1-Poly-6-Metal (1P6M) CMOS technology with deep n-well option [10]. The peak efficiency reached was 73.6% with an output power of 348 µW. Same as in the previous publication, a fully integrated charge pump was used to boost the input voltage and using a Voltage Controlled Oscillator (VCO) controlled by an MPPT circuit. The MPPT used was also the Perturb and Observe algorithm. The main difference and advantage over [75] is that the MPPT monitors the output voltage of the charge pump rather than the output current. Voltage sensing is less energy consuming than current sensing thus resulting in higher efficiency. The input voltage range is 0.21 V to 0.65 V whilst the output voltage range is 0.6 V to 1.8 V. A regulator is required to regulate the output voltage. The maximum power handling of the circuit is 1 mW [10].

A publication detailing the design of a self start-up boost converter with MPPT function for Thermoelectric Energy harvesters is investigated in [76]. The firing circuit consists of a transformer and a low supply voltage transistor having a negative threshold voltage of −15 mV. This transistor is switched on and off with thermal noise across a resistor. Some of the energy is transferred to the secondary coil and resonates with a capacitor thus creating oscillations. This circuit starts up

at a voltage of 40 mV at which the output voltage reaches just 1.2 V. The target output voltage is regulated at 2 V. The MPPT algorithm used in this circuit is the fractional open circuit voltage algorithm. The input voltage range of this circuit is 40 mV to 300 mV whilst the output voltage range is from 1 V to 1.2 V. The peak efficiency reaches 61% at the maximum input voltage of 300 mV. The target output voltage of 2 V is reached with an input voltage higher than 100 mV [76].

Another paper explains the design of a re-configurable charge pump having no on-chip inductors but is capable to adapt the conversion ratio and switching frequency to match the impedance of the charge pump and obtain the MPPT function [11]. The MPPT employed is the perturbation and observation algorithm. The input voltage range of the charge pump is from 0.45 V to 3 V whilst the output voltage is 3.3 V. It is compatible with various types of harvesters including photovoltaic, thermoelectric, and piezoelectric energy harvesters. The charge pump starts with a conversion ratio of 8 and it steps down until the peak value of V_{OUT} is reached. The lowest possible conversion ratio of the charge pump is $1\frac{1}{3}$. For each step, a constant on-time scheme is employed and a SH circuit continuously records the value of V_{OUT}. Once the peak value is reached and the output voltage starts falling again, the step is locked and the MPPT sweeps the switching frequency from 20 kHz to 1 MHz to track the optimal voltage. This circuit was implemented using the 0.18 µm CMOS technology. The throughput power can reach 50 µW and the peak efficiency is 89% [11].

A list of important parameters and details of the work published and reviewed in the state-of-the-art of power conditioning circuits are listed in Table 2.1.

	Harvesting Method	Input Voltage	Output Voltage	Power	Efficiency	Technology	Controller Power Loss	Comments
[61]	Piezoelectric	1.8V-6.5V	N/A	254 µW	95%(MPPT only)	0.35 µm CMOS	N/A	Energy Adaptive MPPT which switches on and off the load. Single stage scheme; active and passive rectifier and capacitor only with no converter implementation
[62]	Electrostatic	5V-60V	2V-5V	25 µW-1.6mW	89% (exc. rect.)	0.25 µm BCD	5uW	PO MPPT, requires externally connected rectifier and load battery
[63]	Electrostatic	<60V	2V-5V	25 µW-1.6mW	89% (exc. rect.)	0.25 µm BCD	5uW	PO MPPT, requires externally connected rectifier and load battery
[64]	Electrostatic	5V-60V	0V-5V	1 µW-1mW	85% (exc. rect.)	0.25 µm BCD	500nW	PO MPPT, requires externally connected rectifier, two resistors, two capacitors and inductor
[65]	Piezoelectric	1V-7V	1V-8V	33 µW-10mW	80% (exc. rect.)	0.35 µm BCD	N/A	Fractional O/C voltage MPPT which operates harvester at half Voc but this is not always correct
[24]	Solar	N/A	N/A	5mW-400mW	90%	Integrated	300 µW	Maintains same voltage irrespective of power. Only suitable for one particular solar cell model
[67]	Solar&Thermal	N/A	2.8V	621 µW	76%	Discrete	135uW	Boost Converter
[68]	Piezoelectric	N/A	3V	8.4mW	72%	Discrete	5.74mW	PO MPPT, Lossy microprocessor controlled, uses shunt resistor to measure current
[69]	Solar	N/A	N/A	1.9W	N/A	0.35 µm CMOS	N/A	PO MPPT
[70]	Solar	1.5V-5V	0V-4V	800 µW	84%	0.35 µmBCDMOS	4.6 µW	PO MPPT, voltage and current sensing using shunt resistor, buck converter only reduces voltage
[71]	Piezoelectric	0.9V-4.2V	1.4V-5V	32 µW	N/A	0.35 µm CMOS	N/A	Rectification by means of an AC-DC voltage doubler, PO MPPT by switching loads (energy adaptive MPPT)
[72]	Thermoelectric	0.5V	2.8V	5.6mW	80%	Discrete	250 µW	No MPPT just impedance setting using Buck Boost meaning circuit needs retuning when changing TEG model
[73]	Solar	1V-2.7V	2V	80 µW	86%	0.35 µm CMOS	850nW	PO with voltage sensing only, charge pump with no energy storage
[74]	Solar	N/A	1V/1.8V/3V	1 µW-10mW	83%	0.18 µm CMOS	400nW	PO MPPT with buck-boost
[75]	Solar	2.1V-3.5V	3.6V-4.4V	780 µW	67%	0.35 µm CMOS	>10 µW	PO MPPT with current sensing and charge pump
[10]	Solar&Thermal	0.21V-0.65V	0.6V-1.8V	<1mW	74%	0.18 µm CMOS	0.74 µW	PO MPPT with charge pump, no energy storage
[76]	Thermal	40mV-300mV	2V	N/A	61%	0.13 µm CMOS	N/A	PO MPPT with transformer boost
[11]	Multiple	0.45V-3V	3.3V	<50W	89%	0.18 µm CMOS	N/A	PO MPPT tuned to match energy harvesting model. Capacitive charge pump

Table 2.1: State of the art of MPPT power conditioning circuits

2.3.2.1 Maximum Power Point sensing circuitry

Maximum Power Point Tracking (MPPT) continuously calculates the power being generated or extracted from the energy harvester. In order to calculate the power value, the voltage and current readings need to be known. In various publications, the MPPT senses both the voltage and current values. Although this is the easiest approach, it is not the most efficient especially since current sensing achieved by means of a resistive shunt converting the current flowing into a measurable voltage, consume a substantial amount of power. Several MPPT designs for low power energy harvesters try to eliminate the need of current sensors to save energy which is highly limited in such applications. Some MPPTs are designed specifically for a particular energy harvester in which their maximum power is achieved at a voltage level which is somewhat constant for various operating conditions [66, 67, 72]. This approach is mostly implemented in solar cells and thermo-electric generators where neither voltage nor current sensors are required in such cases. Although the MPPT is not very accurate, the energy saving by not employing the real MPPT function may lead to additional available energy. However, this approach cannot be replicated onto energy harvesters other than those which have the same characteristics, and which have a constant maximum power point voltage depending on their operating conditions. Moreover, the MPPT must be configured for every energy harvester model.

Power conditioners with the real MPPT function usually use both a current and a voltage sensor to calculate the power being generated by the energy harvester [70]. The only issue is that these sensors add to the power losses of the energy harvesting system especially the current sensor which inevitably has to have some type of series resistance to convert the current being measured into a voltage value. Some MPPT publications tried to calculate the power by using as few sensors as possible to save the limited energy available in energy harvesters. Consequently, a paper which reports a Buck-boost converter, operating in DCM only uses a current

sensor to determine the extracted power. This is because the power being handled by a Buck-boost converter operating in DCM can be calculated from the current, duty cycle, switching frequency and inductance value of the inductor [68]. Another MPPT power conditioning circuit designed to charge a super capacitor or a battery from a solar cell by using only a charge pump, makes use of one current sensor. The MPPT assumed that the output voltage is constant for long periods of time and hence MPP was achieved by maintaining the output charging current as high as possible. This circuit also uses only one current sensor to reach MPP and no voltage sensing is done. Since current is sensed at the output of the circuit rather than at the input, this MPPT also takes in consideration the power overhead within the charge pump and control circuitry itself and calculates the MPP including the overhead losses of the energy harvesting system [75].

Several other MPPT power conditioners preferred to eliminate the current sensor rather than the voltage sensor since it is a high-power dissipating block. MPPT power conditioners for solar cells or piezoelectric harvesters make use of the Fractional Open Circuit algorithm which only requires to sense the voltage at open circuit condition to determine the voltage at which MPP is reached. Consequently when using such algorithm, only one voltage sensor is required thus saving power consumption [65, 71, 76]. An electrostatic energy harvester also used only one voltage sensor to obtain the MPPT function. The publication explains that after taking various assumptions, the power being extracted from the harvester can still be calculated [62, 64, 63]. A vibration energy scavenging system makes use of a voltage sensor just to sense the vibration status; magnitude and frequency from which it determines the voltage at which maximum power can be obtained. However, this MPPT can only be used for this type of harvester [61].

Other MPPT types developed for low voltage energy harvesters are reported in [10, 11]. In both cases, a charge pump having the MPPT function by targeting their output voltage to be as high as possible. This made use of just one voltage

sensor at the output thus minimising the power loss. The only issue in these circuits is that any excess energy from the harvester cannot be stored since it just controls the output voltage to be as high as possible. If the power being fed to the load is lower than the maximum power which can be extracted from the harvester, increasing the output voltage does not make use of the excess power being scavenged. Having another block to store energy is ideal so that when no power is being generated from the harvester, the energy stored can be supplied to the load to get less interruptions in the operation of the loads.

2.4 State of the Art Integrated Regulating DC-DC Converters

Stepping down an input DC voltage is typically achieved using either linear regulators or switch-mode converters. The former is very inefficient especially at high voltage conversion ratios [77]. Switch-mode DC-DC converters can convert DC voltages by temporarily storing the energy and then releasing it at a different voltage level. Several converter topologies capable of voltage step-down exist such as Buck converter, Buck-Boost converter, Flyback converter and Half bridge converter. Improvements on switch mode DC-DC converters involves synchronous switching, where the freewheeling diode is replaced by a transistor to obtain a higher efficiency as long as the converter remains operating in the CCM. However, when synchronous switched converters operate in DCM, the efficiency is worsened because the inductor current goes negative unless a zero current detector circuit is implemented [78]. Most DC-DC converters are close loop controlled where a constant output voltage can be obtained from a wider range of input voltages and output load current conditions [79, 80]. A closed loop control loop is usually designed on a converter operating in CCM so that its stability is maintained even if the converter shifts to DCM. A control loop tuned for a converter set to operate

in DCM may become unstable if it shifts to CCM [81]. Most converters especially those implemented using discrete electronics are operated via PWM at a fixed switching frequency, which require the use of an oscillator to generate this switching frequency. However, in low power applications such as integrated converters for energy harvesting applications, the power consumption introduced by such an oscillator can be too high in comparison to the power available from small energy harvesting devices. In such applications, hysteretically controlled converters may sacrifice the output ripple voltage so that the power dissipation introduced by the oscillator is eliminated. In some designs as in [82], even hysteretic controlled converters, use an oscillator, thus still increasing the power consumption of the control circuitry.

Although hysteretic control may result in a higher ripple voltage present in the output, its design technique still has some advantages over PWM control. Hysteretic control of a switch-mode converter is mostly used to obtain a faster transient response, lower power dissipation in the control circuitry, a simpler control design and simplification of the modelling of the steady state equations and dynamic analysis [83].

The simplest step-down converter topology is the Buck converter because it requires the least number of components; one switching transistor, one freewheeling diode, one inductor and one capacitor. However, the switching device is on the high side and so this must be implemented either by using a PMOS transistor or by using an NMOS transistor driven by a bootstrapping circuit. High voltage PMOS transistors with a thin gate oxide layer (to be driven with a low V_{GS}) are not available in several high voltage technologies [84]. For this reason, the only solution to implement a switching device on the high side is by using an NMOS transistor driven by a bootstrapping circuit. A capacitively coupled bootstrap circuit was implemented using discrete components in [85]. Such circuit is ideal when there is a substantial voltage difference between the control supply voltage and the converter's input

voltage.

2.5 Conclusion

Following a thorough review of the state-of-the-art, it was found that the single stage scheme and the two-stage schemes investigated in [7] both make use of either a passive or an active rectification stage. The single stage scheme which consists of just a rectification block directly charging a storage capacitor as shown in Figure 2.2, does not offer an MPPT function. The two-stage scheme which consists of a rectification stage and a converter as shown in Figure 3.2, can offer the MPPT function but however the two separate subsequent stages both incur losses which reduce the total efficiency of the power conditioning circuit. If the rectification block in the two stage scheme is replaced by an AC/DC-to-DC converter controlled by an MPPT as proposed in this work, more energy can be generated from the same energy harvester. Moreover, having the rectification included in the converter, can achieve higher conversion efficiency.

From the review of the state-of-the-art of power conditioning circuits, all the publications investigated are designed to work only with a particular energy harvesting method. For example [61, 65, 71] report power conditioning circuits designed to work with piezoelectric energy harvesters, whereas [69, 24, 73, 74, 75, 10] report power conditioning circuits designed to work with solar cells and [72, 76] are designed to work with thermo-electric energy harvesters. Furthermore, several power conditioning circuits are designed to work with only a particular energy harvesting model such as [66] which can only work with a particular solar cell model. This is a limiting factor of all the power conditioning circuits investigated listed in Table 2.1. Even the input voltage and power ranges are narrow thus compatibility to energy harvesters is very limited. If a power conditioning circuit is capable of working with both DC and low frequency AC (up to kHz range), then

all the energy harvesting methods except for RF can work with the proposed work.

Due to the power consumption constraints of this application, the MPPT circuit was implemented using analogue electronics techniques using simple and power efficient circuit designs. An interesting aspect investigated is a controller capable of reaching MPP by only sensing the output voltage as in [10, 11] and therefore there is no need of current sensing which is a high power dissipating block. Moreover, having just one input, the controller does not require multipliers which may add further power dissipation during normal circuit operation. Several direct AC/DC-to-DC converter topologies investigated in the state-of-the-art are compared in further detail in Section 3.1 to determine the most practical converter topology for this application.

Some of the maximum power point tracking algorithms investigated cannot work with energy harvesters with unknown specifications and require adjustment depending on the specifications of the energy harvester connected to the power conditioning circuit. This makes them unsuitable to MPPT power conditioning circuits designed to work with different energy harvesting devices.

Energy harvesters generate a variable output voltage and power depending on the current operating conditions. Therefore, the output voltage to supply the load needs to be regulated. A simple, effective design is hysteretic controlled buck converter which doesn't require any oscillators to generate the pulse width modulation. Driving the high side transistor of a buck converter can prove challenging and has to be done by means of a bootstrapping circuit.

3. Proposal of a Novel Power Conditioning Circuit

Following a thorough review of the state-of-the-art presented in Chapter 2, a proposal of a novel power conditioning circuit was drafted to address the gaps emerging from the review. A block diagram of the novel power conditioning circuit is given in Figure 3.1 [6]. This chapter presents a preliminary study based on system level simulations which were carried out to verify the feasibility of the proposed architecture. The proposed power conditioning circuit is divided into two stages: energy from the harvester is initially stored in a high storage capacitor by means of a switch mode converter being controlled by a Maximum Power Point Tracking controller (Block MPPT Converter) and then the voltage across the storage capacitor is regulated by means of a DC-DC converter prior to feeding it to the load.

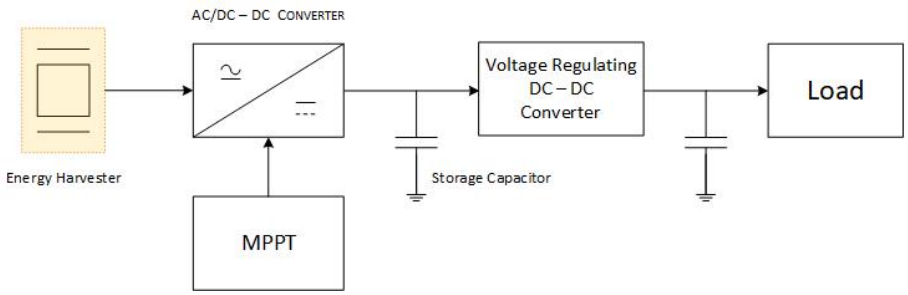

Figure 3.1: Block diagram of the proposed power conditioning circuit.

This is a different approach from the two schemes investigated in [7]. Single stage schemes only utilise a full wave rectification stage either using passive or active rectification. Two stage schemes as proposed in [8, 9] (refer to Figure 3.2) consist of a full wave rectification stage, using either passive or active rectification, a temporary storage capacitor and a DC-DC converter to generate a regulated output voltage.

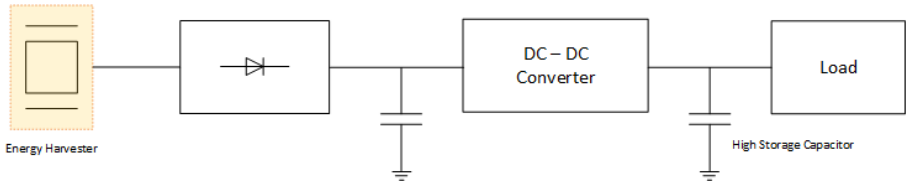

Figure 3.2: Generalised two stage scheme [7]

The proposed power conditioning circuit designed for energy harvesters is an improvement to two stage schemes by replacing the full wave rectification block by a direct AC/DC-to-DC converter with MPPT function. The high storage capacitor's voltage is expected to reach a voltage of about 50 V at low load conditions. This high voltage can be easily reached since some energy harvesters, such as the piezoelectric energy harvesters, are able to generate a voltage of 15 V at normal vibration levels [23]. Since the initial stage consists of a boost converter, this input voltage will be stepped up even further. The MPPT requires to work within a substantial voltage range so that it operates efficiently, and so a maximum voltage of 50 V at the output of the MPPT converter block is essential. Several integrated circuit technologies feature high voltage transistors which can be safely operated at this voltage level. Another advantage of storing a high voltage in the energy storing capacitor is that the energy storing capacitor is that more energy can be stored in a certain capacitance when using higher voltage, since the stored energy is quadratically related to the capacitor voltage. Moreover, higher efficiency levels can be obtained from a circuit when operating at higher voltages and lower currents due to lower conduction losses. Another innovation in this power conditioning circuit

design is that it can be connected to any type and model of energy harvesting devices if the energy harvester's output falls within the input limits of the circuit. The design is compatible with energy harvesters which produce both a DC output voltage and an AC output voltage at various frequencies and having an input voltage range of up to 40 V. From the state-of-the-art review carried out on power conditioning circuits, all the publications, are designed to work with a particular energy harvesting device. For instance, the converters reported in [61, 65, 71] are power conditioning circuits designed to work with piezoelectric energy harvesters, whereas those presented in [69, 24, 73, 74, 75, 10] are power conditioning circuits designed to work with solar cells and those in [72, 76] are designed to work with thermo-electric energy harvesters. Furthermore, several power conditioning circuits are designed to work with only a particular energy harvesting model such as [66] which can only work with a particular solar cell model. The novelty of the proposed power conditioning circuit is that it can work with piezoelectric, pyroelectric, photo-voltaic, electromagnetic, electrostatic, and thermoelectric energy harvesters and operate all energy harvester types and models at maximum power point due to the MPPT algorithm adopted. In the literature review, several passive and active rectification circuits were analysed, with active rectification being identified as the most efficient. However, several converter topologies were found to be able to both rectify and boost the voltage concurrently. Although having a separate rectifier and converter has the advantage of simplifying the design and allowing for a better analysis and control of the circuitry, the operating efficiency in this work was considered paramount because the power conditioner is targeted for microwatt and milliwatt range energy harvesting applications. Such a low power is easily lost in switching losses, conduction losses and control circuitry. Therefore, particular attention and decisions were taken at all design stages to choose the least complicated options with minimal energy losses. Therefore, this design opted to use a direct AC/DC-to-DC converter instead of using a separate initial rectification block to convert AC inputs from piezoelectric, pyroelectric, electromagnetic and

electrostatic generators to DC, and thus the proposed conditioning circuit should be capable of reaching higher efficiency levels. The goal of this work was to integrate most of the circuitry including the converter and control circuits except for a single inductor and a single high storage output capacitor. As emerged from the literature review, the proposed converter topology was never implemented in an integrated circuit before. The controller is capable of reaching MPP by sensing only the output voltage as proposed in [10, 11] and therefore there is no need of a multiplier and a current sensing stage which are a highly demanding in power. All the control circuitry is implemented using analogue electronic techniques to get higher efficiency, since microprocessors, ADCs, DACs and clock generators consume a substantial amount of power, which is sometimes higher than the power available from energy harvesters. Additionally, all transistors in the control circuit are operated in the sub-threshold region to limit the current flowing through the transistors, thus further reducing the power dissipation. The final stage of the proposed power conditioner consists of another DC-DC converter to step down and regulate the capacitor's voltage to normal operating voltages such as 1.8 V, 3.3 V and 5 V, as required by typical electronic circuits. This part of the circuit also generates the required voltages to power the control circuitry of all the power conditioning circuit. The converters in this part of the power conditioning circuit are hysteretically controlled to maintain the control power dissipation to a minimum. An innovative approach is the ability to compromise between output ripple voltages, and the control power dissipation. The output voltages of all three converters are settable via an external feedback resistor and a feedback capacitor can also be implemented to lower the startup output voltage overshoot. A bootstrapping circuit was implemented to drive the high side NMOS transistor in the synchronous Buck converter. This bootstrapping circuit which is capacitively coupled because of the voltage difference between the control and the power circuitry, will be the first time which such a circuit is implemented on-chip [85]. The design, simulations and circuit characterisation are explained in

Chapter 5.

3.1 AC/DC-to-DC Converter with MPPT

3.1.1 AC/DC-to-DC Converter Topology

A thorough research was carried out to identify the most suited converter topology for this application and which is implementable in the MPPT converter, which is the first stage in the power conditioner architecture. All the issues and advantages of the topologies were backed by preliminary simulations carried out using the Plexim PLECS software. Five direct AC - DC switch mode converter topologies mentioned in the literature review were considered. All five converters had their operation analysed in detail.

The AC - DC converter shown in Figure 2.8 is a combination of a boost converter for the positive half cycle and a buck boost for the negative half cycle. A major disadvantage of this topology is that it can only operate at input voltages lower than the threshold forward voltage of the parasitic diodes in the MOS transistors. When considering that the power conditioner handle voltages up to 50 V, this topology cannot be implemented for this application. Another disadvantage of this topology is that to operate the boost converter and the buck boost converter, fully independent control systems are required as the transfer functions of the converters are different. Additionally, this converter topology requires an inductor for each converter. Polarity sensing and zero crossing circuits are also essential so that the respective converter is operated depending on the current half cycle. This increases the complexity which in turn creates further losses in the control system of the power conditioning circuit. The components required in this topology are two switching transistors, two diodes, two inductors and an output capacitor. The source of the switching transistor of the Buck Boost converter is not connected to ground. This further complicates the operation of the converter as a high side

charge pump gate driver would be required to drive this transistor.

The standard version AC - DC converter shown in Figure 2.6 consists of a single inductor, two diodes, a single capacitor and four switching devices. Two of the switching devices are a PMOS and an NMOS which create a bidirectional boost switch. These switches are switched on and off simultaneously and irrespective of the input voltage polarity. The secondary side switches are switched on and off according to the polarity and with the same frequency of the input voltage. Hence polarity sensing and zero crossing circuits are necessary for this topology. Also, a total of four gate drivers are required in order to switch on the four transistors. An improved simplified version of this converter is the split-capacitor converter which replaces the secondary side transistors with two capacitors [52]. The low number of components makes this topology one of the simplest and most efficient. This improved version now eliminates the need to sense the polarity of the input voltage to control the converter accordingly which makes it simpler and more efficient to operate. However, a disadvantage of the split-capacitor topology over the original version is that each of the output capacitors is charged only for one half cycle of the energy harvester. Therefore, this converter topology tends to have larger ripple voltages across its output than in other types of converters. Therefore, to maintain the voltage ripple within an acceptable limit, a large output capacitor is needed, which in most cases is impractical due to the size restrictions in practical uses of such power conditioning circuits. Moreover, a large output capacitor slows the converter's response time. [52].

Two versions of the dual Boost AC to DC Direct converters exist. The standard version as shown in Figure 2.5 requires two switching devices, two diodes and two inductors. Polarity sensing and zero crossing circuits are a requirement for the correct operation of the boost converters. An issue with this standard dual boost version is that it can only work when the maximum source voltage is less than the threshold forward voltage of the parasitic diodes in the MOS transistors. This

	Voltage restricted due to parasitic diodes in mosfets	Further Comments
Combined Boost and Buck-Boost	Yes	
Standard Dual Boost	Yes	High Ripple
Improved Dual Boost	No	May be Lossy
Secondary Side Switch-based Boost	No	Lossy PMOS and NMOS gate drivers required
Split Capacitor Version Boost	No	High Ripple PMOS and NMOS gate drivers required

Table 3.1: Comparison of restrictions and disadvantages in various Direct AC - DC converter topologies

topology was then improved so that only one capacitor and one inductor are needed, as shown in Figure 2.7. In some cases, the inductance required can be obtained by the parasitic inductance of the energy harvester. Although this improved topology can work with voltages higher than the threshold forward voltage of the parasitic diodes in the MOS transistors, the current needs to pass through the parasitic diode of the switching device of the non-operational boost converter in order to complete the loop. This incurs an additional voltage drop which results in additional power loss.

Table 3.1 lists the restrictions and disadvantages of all five converter topologies considered for this application. Since the proposed power conditioner is required to work with voltages of up to 50 V, which certainly exceeds the forward voltage of the parasitic diodes in the MOSFET switching devices, the Combined Boost and Buck-boost AC - DC direct converter and the Standard Dual Boost AC - DC direct converter were excluded. The remaining three converters all have their advantages and disadvantages. In order to keep the conversion losses to a minimum, the operation of the converter should be as simple as possible. High side gate drivers, PMOS and NMOS gate drivers, polarity sensing and zero crossing detecting circuits all incur an additional power dissipation. The additional circuitry required for every converter topology considered for this application, are listed in Table 3.2.

It was comprehended that both switching devices, in the improved version of dual boost direct AC-DC converter, can be switched on simultaneously. This means

	High Side Gate Driver	**Polarity & Zero Crossing Sensing**	**Independent Control**
Combined Boost and Buck-Boost	Required	Required	Required
Standard Dual Boost	No	Required	No
Improved Dual Boost	No	No	No
Secondary Side Switch-based Boost	No	Required	No
Split Capacitor Version Boost	No	No	No

Table 3.2: Comparison of required blocks for correct operation in various Direct AC - DC converter topologies

	Inductors	**Capacitors**	**Diodes**	**Switching Devices**
Combined Boost and Buck-Boost	2	1	2	2
Standard Dual Boost	2	2	2	2
Improved Dual Boost	1	1	2	2
Secondary Side Switch-based Boost	1	1	2	4
Split Capacitor Version Boost	1	3	2	2

Table 3.3: Comparison in number of components required in various Direct AC - DC converter topologies

that this converter topology does not require any of the above-mentioned circuits. The only disadvantage in this converter is that the inductor current must pass through two switching devices at all times which may add to the conduction losses. However, since the switching devices are switched on simultaneously, the losses in the parasitic diode will be substantially lowered during the on cycle because both devices will be switched on concurrently.

Table 3.3 lists the active and passive components required for every converter topology considered for this application.

The secondary side switch-based Boost direct AC-DC converter requires polarity sensing and apart from two diodes, requires four switching devices which all need to have an independent gate driver. Two of the switching devices are PMOS transistors which when considering an operating voltage as high as 50 V complicates matters in the design of their respective gate driving circuits.

The secondary side split capacitor version Boost direct AC-DC converter does not require any charge pump gate drivers and polarity sensing. However, one of the switching devices needs to be a PMOS transistor thus complicating the design of

its respective gate driving circuit when considering an operating voltage.

Hence when taking in consideration all the control blocks and disadvantages of the converter, the most efficient and practical converter in this application is the Improved Dual Boost direct AC-DC converter. This converter was never implemented as an integrated circuit and this work is the first instance where this converter topology is being included on-chip.

3.1.2 Maximum Power Point Tracking Algorithm

The MPPT algorithm had to be compatible with all energy harvester types which can be connected to the proposed power conditioning circuit. Furthermore, the power dissipation of the circuit implementing this algorithm must be as low as possible. The whole converter together with its control system are implemented in analogue rather than in digital. Digital circuits are capable to carry out much more complex calculations and control, but they would require a processor, Analogue to Digital converters (ADCs) and Digital to Analogue converters (DACs) in order to work. These digital circuits typically consume a substantial amount of power, sometimes consuming all the power being generated from the energy harvester, leaving no available power for the microwatt and milliwatt loads to be connected. Hence to avoid losing this amount of power, all the control is implemented in analogue electronics. Therefore, the MPPT algorithm to be chosen had to be simple enough so that it is possible to implement it in analogue electronics and with the minimum number of blocks and transistors possible. On the other hand, the MPPT is a crucial part of the power conditioner and must be trustworthy and efficient.

The MPPT requires enough information to calculate the voltage at which to operate the energy harvester to extract the maximum power possible. The more inputs available, the easier it is for the MPPT to calculate the MPP. However, each input

will incur a power loss and these still should be kept to a minimum. Moreover, the inputs have to be processed and additional blocks such as multipliers would be necessary. From the literature review, two converters with the MPPT function were being operated by sensing only the output voltage [10, 11]. Utilising only a voltage sensor eliminates the requirement of both a current sensor and a multiplier. Voltage sensing dissipates less power than current sensing which is advantageous in this application. Hence an MPPT operating with only one voltage sensor is the most efficient MPPT circuit one could attain. If the load connected to the power conditioning circuit is nearly constant for most of the time and varies at a rate slower than the response of the converter, the MPPT will then adjust the converter's operating voltage to keep the output voltage of the converter at the maximum voltage possible. This is ensured by the high capacitance of the storage capacitor connected to the output of the converter. Any power or current demand bursts by the load is further filtered by the high capacitance of the output capacitor. This ensures that maximum power is extracted from the energy harvester and the rate of change of the output voltage is kept limited. Moreover, since the voltage is being measured at the converter's output, the MPPT even takes into consideration the losses in the converter itself.

As previously explained in Section 2.3.1, there are four maximum power point tracking techniques; the Fractional Open Circuit Voltage Algorithm, the Fractional Short Circuit Current Algorithm, the PO Algorithm or SH and the Incremental Conductance Algorithm. The proposed power conditioning circuit is designed to operate with various types and models of energy harvesters. The controller will not have any information whatsoever on the type and model of the energy harvester that is connected at its input. The fractional open circuit voltage algorithm would require that the circuit is preset with the constant between the open circuit voltage and the voltage at which maximum power is achieved. Similarly, the fractional short circuit current algorithm would require that the circuit is preset with the constant

between short circuit current and the current at which maximum power is achieved. And this assumes that this constant does not change with the operating conditions of the energy harvester. In this case, a lookup table needs to be used and the MPPT circuit cannot be implemented in analogue electronics. Since the power conditioning circuit is not intended to be preset according to the properties of the harvester being connected to it, these two algorithms were not considered. Both the perturbation and observation and the incremental conductance algorithms could in theory be adopted in this power conditioner. Preliminary simulations were carried out to help deduce the most efficient algorithm.

3.1.2.1 Perturbation and Observation MPPT Algorithm Simulations

The Perturbation and Observation MPPT algorithm can be easily implemented in analogue electronics by using a SH circuit and a comparator. Figure 3.3 shows the main schematic of the simulation of the PO algorithm. As an input, a micro-watt energy harvester was simulated with an AC voltage source having a series capacitance, a series resistance and terminal capacitance, representing the internal impedance of a typical piezoelectric energy harvester.

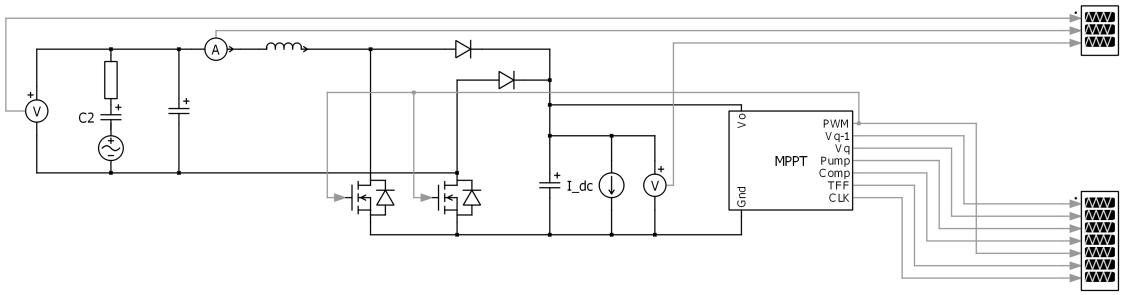

Figure 3.3: Main Schematic of Perturbation and Observation MPPT Algorithm

The chosen topology, which is the single inductor improved dual boost direct AC/DC-to-DC converter, is also included in the simulation. Since this converter does not require polarity sensing and the transistors conduct current together, the gate connections of both transistors are tied together and driven by the same gate

driver irrespective of the polarity and current direction. The converter then stores the energy in the output high storage capacitor at a higher voltage. A constant current source was connected at the output to simulate a load of the output.

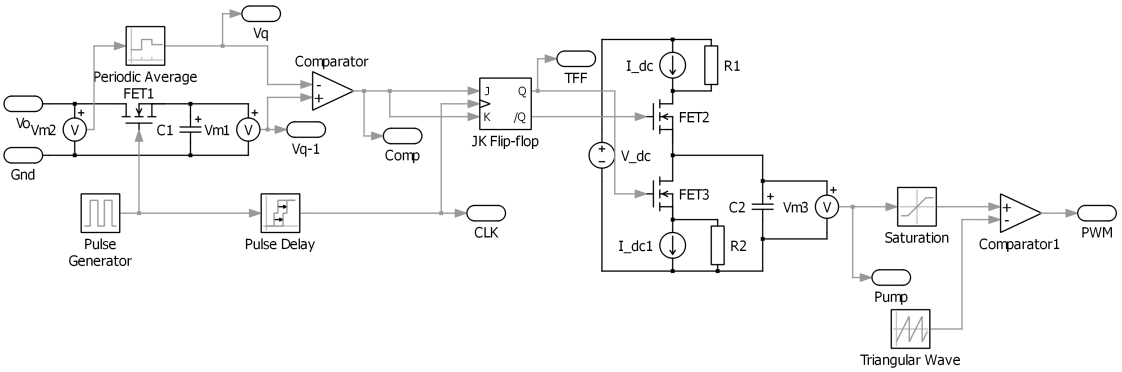

Figure 3.4: Simulation setup of the MPPT, Control and Gate driver of PO Algorithm in Plexim PLECS

Figure 3.4 shows the PO MPPT, control and gate driver that from the output voltage, operates the dual boost converter. The control was kept as simple as possible. The SH runs at a clock rate of 15 Hz. The clock frequency of the MPPT control was chosen after simulation parametric analysis of the converter's operation. The frequency should be slow enough to allow enough time for the converter to settle to the changing duty cycle. Since the output of the converter is intended to be a high storage capacitor, the settling time is quite slow leading to a low clock frequency required to operate the control loop. When this clock frequency is too fast, the MPPT would alter the duty cycle towards a lower power point rather than towards maximum power point. This clock is generated by the pulse generator. The comparator compares the actual filtered output voltage with the output voltage in the previous cycle stored in the sample and hold's capacitor. If the actual voltage is lower than the previous voltage, then the TFF would change state. The TFF was implemented by shorting the J-K inputs of a J-K Flip Flop. Depending on the TFF state, a charge pump either increases or decreases the capacitor's voltage. The capacitor is part of the charge pump. This is achieved by switching

on the pull-down transistor when the TFF's state is High and switching on the pull-up transistor when its respective state is Low. The capacitor's voltage would then determine the duty cycle at which the gate driver operates the converter's switching devices. A switching frequency of 200 kHz was applied to the converter in the simulation. Most of the time, the converter's operation is in Discontinuous Conduction Mode (DCM). Hence a high switching frequency is beneficial to enable more power transfer through the converter. However, a compromise had to be reached since high switching frequencies would mean more power dissipation due to the gate charging and discharging in the power transistors and higher switching losses in the power transistors and diodes of the converter. Most of the component sizing and clock frequencies were still premature in the simulation because the simulation was actually used to determine which MPPT algorithm to adopt in the power conditioner being designed rather than determining the exact specifications of the circuit.

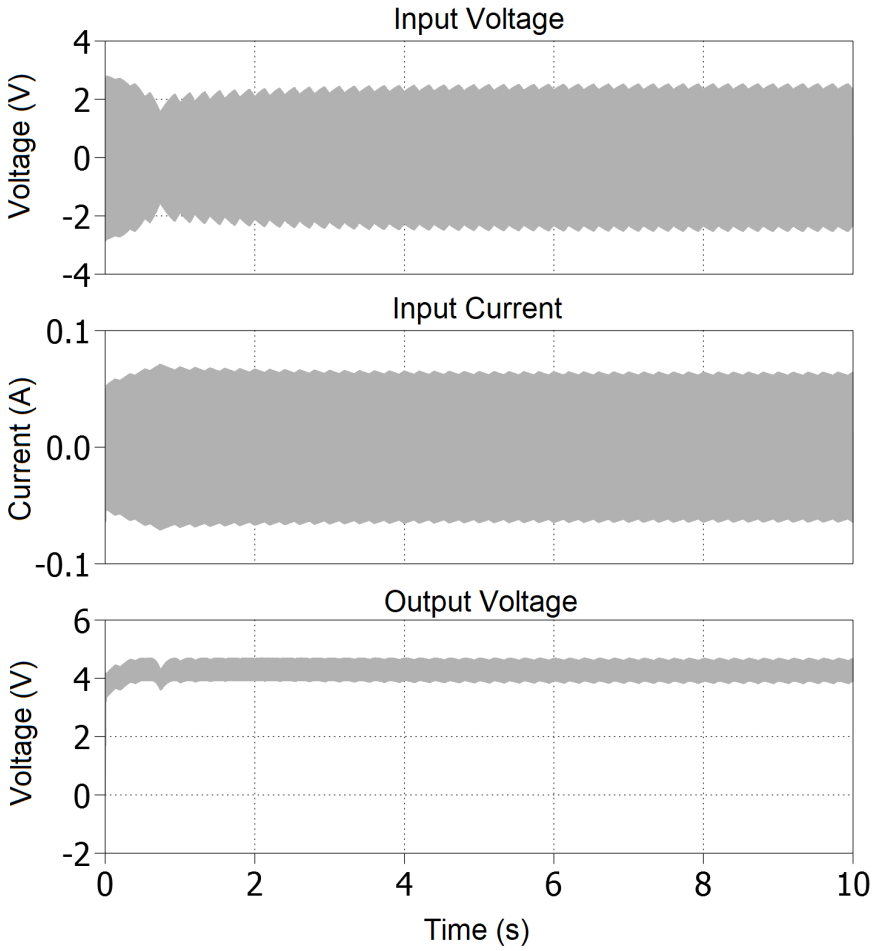

Figure 3.5: Simulation results of Converter's Voltages and Current when operating under PO Algorithm

Figure 3.5 shows the input voltage, input current and output voltage of the Dual Boost converter when operated under the PO MPPT algorithm.

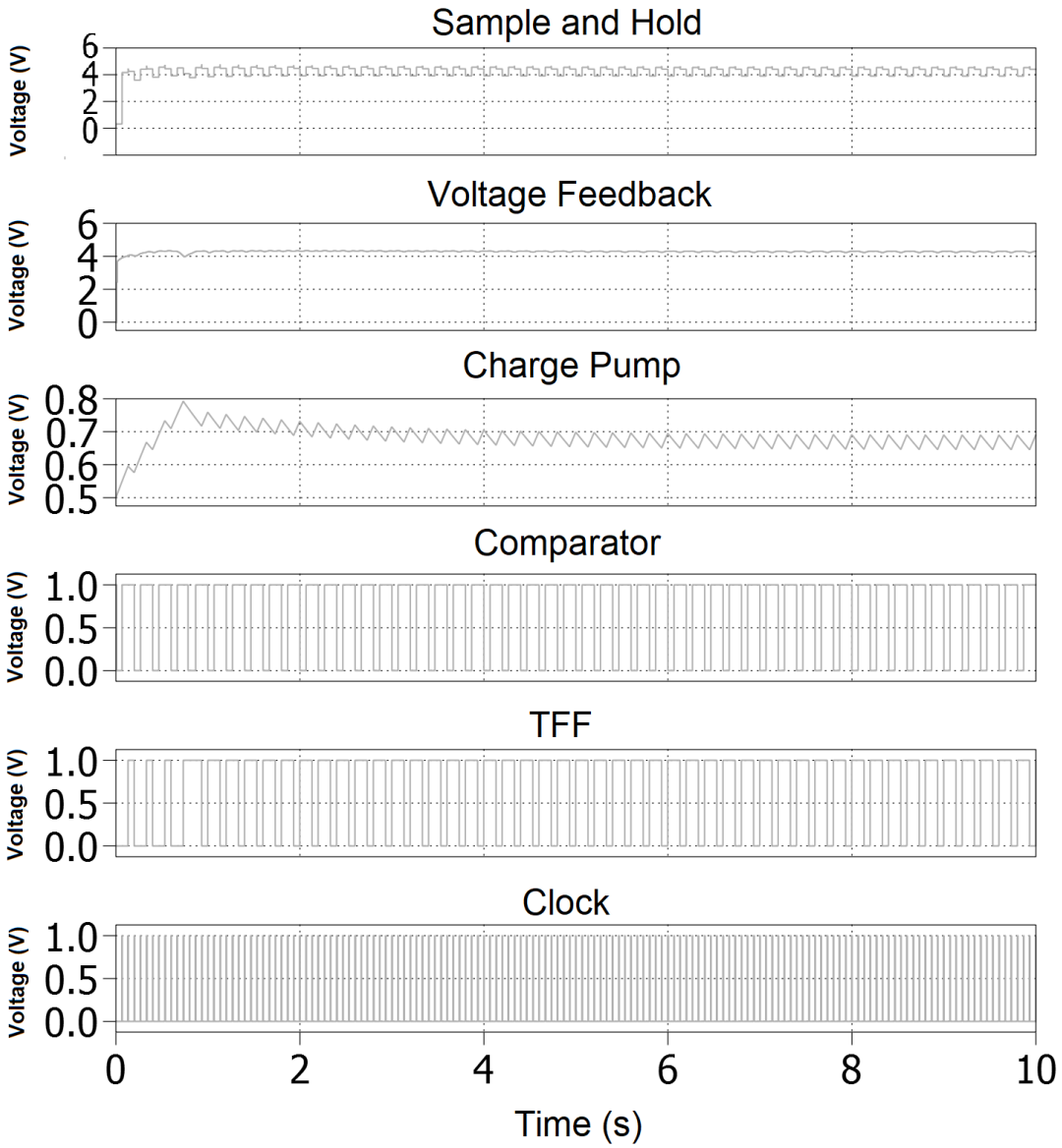

Figure 3.6: PO MPPT control and Gate Drive simulation results

Figure 3.6 shows the simulation results and the operation of the control and gate drive circuits. SH signal shows the output from the SH circuit while the Voltage Feedback trace shows the actual output voltage which is slightly filtered to eliminate the ripple generated from the switching converter. The Comparator trace shows the output of the comparator which is comparing the current output voltage with

the previous output voltage. The TFF signal shows the state of the TFF which changes when the comparator's output is high during the clock pulse shown in Clock signal. The charge pump capacitor's voltage shown in signal labelled Charge Pump is increased and decreased depending on the TFF's state. The duty cycle of the Pulse Width Modulation (PWM) gate driver is determined by the output voltage of the charge pump.

3.1.2.2 Simulations of the Incremental Conductance MPPT Algorithm

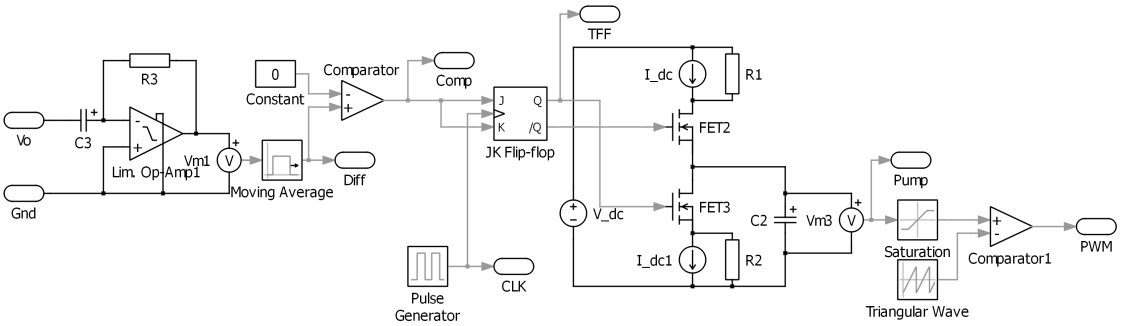

Figure 3.7: MPPT, control and gate driver of Incremental Conductance Algorithm

The incremental conductance MPPT algorithm can be implemented in analogue electronics by use of a differentiator. The same schematic shown in Figure 3.3 with the same components, component sizing and clock frequencies, was maintained in this simulation in order not to affect the output of the simulation by any changes in the converter. The schematic shown in Figure 3.7 shows the Incremental Conductance MPPT, control and gate driver of the power conditioning circuit. This schematic is the same to that shown in Figure 3.4 except for the initial part. The TFF, charge pump and gate drive are the same. The only change is that the SH was replaced by the differentiator.

The derived differentiator transfer function is

$$V_o = -RC\frac{\delta V_{IN}}{\delta t} \tag{3.1}$$

Therefore, an increasing input voltage at the differentiator's input would result in a negative output voltage and a decreasing input voltage would result in a positive output voltage. The output of the differentiator is then compared to zero. If the output of the differentiator is larger than zero (positive), then the output voltage of the converter is decreasing and hence the TFF changes state. If the output of the differentiator is less than zero (negative), then the output voltage of the converter is increasing and hence the state of the TFF is maintained. The initial idea was for the MPPT not to be clocked but this approach has presented a problem. The dual boost converter charges a large output storage capacitor, and this makes its response time slow. Hence if the MPPT is not clocked, this would result in the TFF to keep switching states before waiting for the converter's reaction to the changing duty cycle. Furthermore, another issue was the voltage ripples which unless there is a substantial change in the output voltage, the differentiator would still give some positive values, switching the TFF's state even though the output voltage is increasing slowly. The solution was for the MPPT to be clocked so that enough time is left for the converter to react to the changing duty cycle and for the change in voltage to be substantially higher than the ripple voltages. This MPPT algorithm is clocked at 20 Hz. The clock frequency of the MPPT control was chosen after analysis of the converter's operation in the simulation. The frequency should be slow enough to allow enough time for the converter to settle to the changing duty cycle.

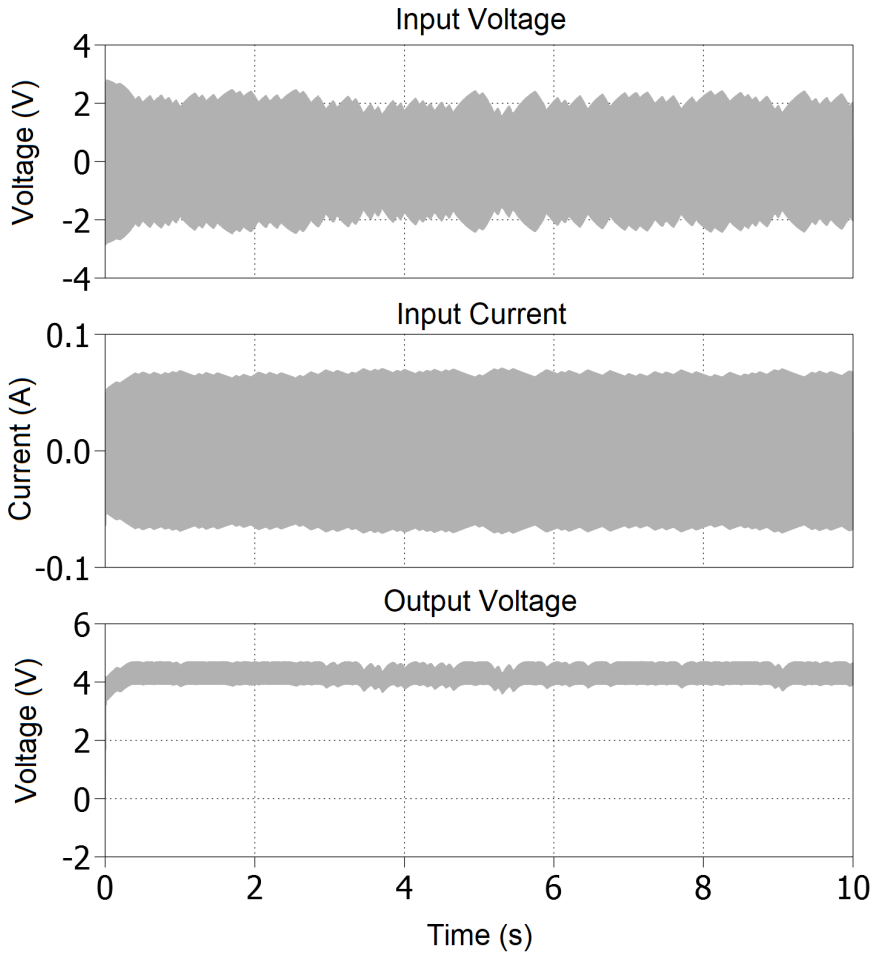

Figure 3.8: Simulation results of Converter's Voltages and Current when operating under Incremental Conductance Algorithm

Figure 3.8 shows the input voltage, input current and output voltage of the Dual Boost converter when operated under the Incremental Conductance MPPT algorithm. It is evident that the voltages and current of the converter operated under the PO MPPT algorithm are more stable than when operated under the Incremental Conductance MPPT algorithm.

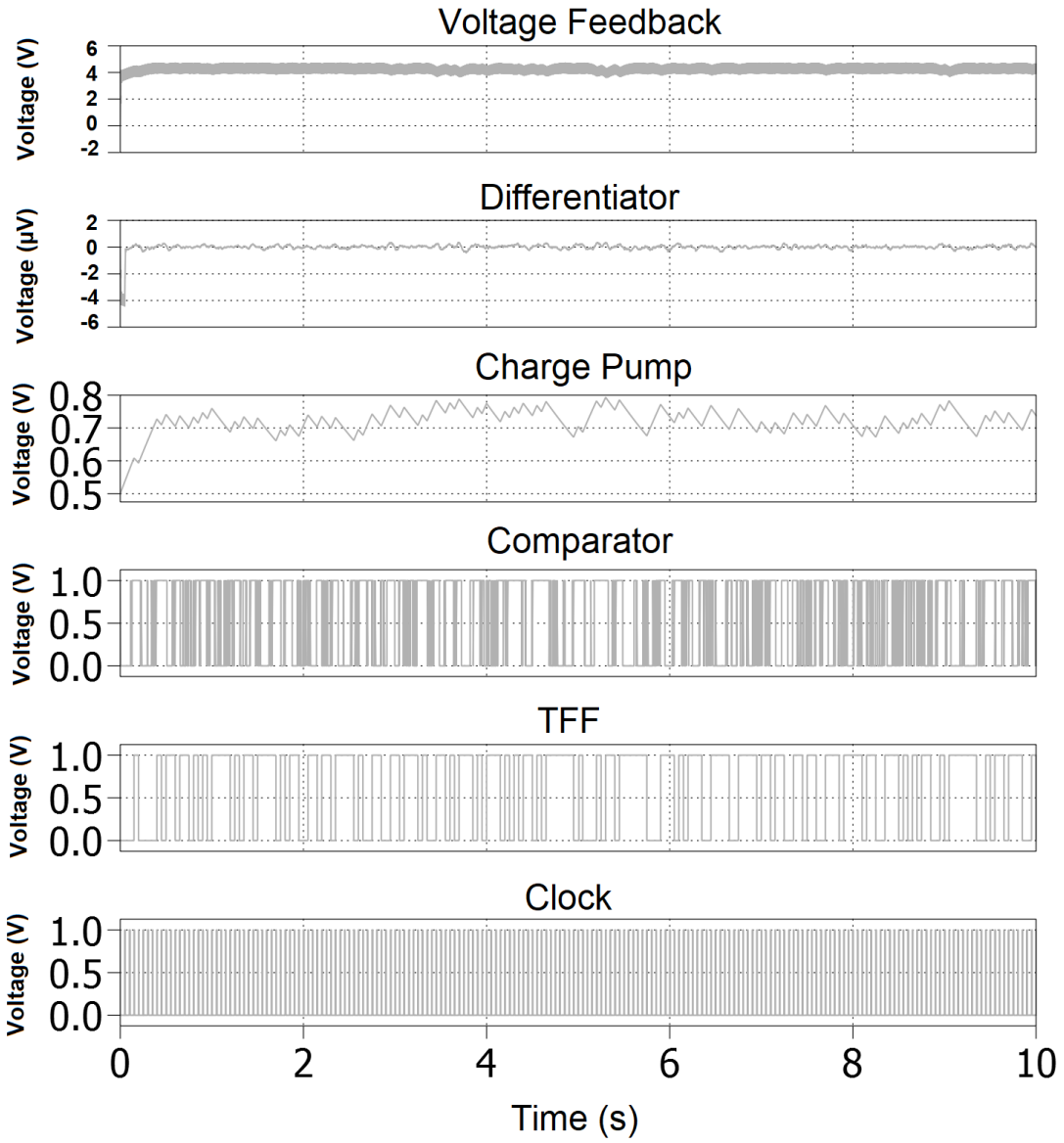

Figure 3.9: Incremental Conductance MPPT control and Gate Drive simulation results

Figure 3.9 shows the signals in the MPPT controller and gate driver. The output voltage of the improved dual boost converter is shown in Voltage Feedback graph. The differentiator's output is represented by the trace labelled Differentiator. The TFF signal shows the state of the TFF whereas the Charge Pump graph shows the voltage of the charge pump's capacitor which determines the duty cycle of

the gate drive at which the switching devices of the Dual boost converter are operated. Both the PO and this MPPT were optimised as best as possible, and the simulation results being presented were the best one could attain. The low voltages and currents involved made it challenging to get a more stable output from both PO and Incremental Conductance MPPT controllers.

When comparing the PLECS simulation results in Figure 3.5 and Figure 3.8 it can be deduced that the PO MPPT operates in a more reliable and stable manner. However, both were designed in Cadence Virtuoso to confirm which MPPT integrated circuit design operates better.

3.2 Hysteretic Regulating Buck Converter

The second stage of the power conditioning circuit consists of an integrated regulating buck DC-DC converter controlled hysteretically. By using hysteretic control, the control circuit does not require an oscillator for the Pulse Width Modulation (PWM) generation and hence lower control power dissipation is achieved. The design of the hysteretic control technique of a buck converter is mostly used to obtain a faster transient response, lower power dissipation in the control circuitry, a simpler design and simplification of the modelling of the steady state equations and dynamic analysis [83].

The high side transistor in the Buck converter can be implemented either using a high voltage PMOS transistor or a high voltage NMOS transistor driven by a bootstrapping circuit. This circuit has to be driven by the lowest possible supply voltage to maintain the control circuit's power consumption to a minimum. However, this can be only as low as the minimum voltage which drives the high voltage transistors. The PMOS transistor having the lowest driving voltage in the X-FAB XH035 technology is the medium thickness gate oxide layer which requires a driving V_{GS} voltage of 5 V. Operating the control circuit at this voltage increases

the power consumption of the control circuit. This also entails that all transistors within the circuit need to be implemented with higher voltage transistors because the normal transistors available in the technology have a breakdown voltage of 3.3 V [84]. Another disadvantage with using a 5 V supply voltage is that the circuit only cold starts when such voltage is available at its input. So, this raises the cold start voltage to a level higher than 5 V which makes all the energy harvesters that generate a lower voltage incompatible with the power conditioning circuit. So, for these reasons, it was decided to use a high voltage NMOS transistor having a thin gate oxide layer which can be driven by a gate voltage of 2 V. This is driven by a bootstrapping circuit which is integrated as part of the circuit. The innovation of the bootstrapping circuit is that it is capacitively coupled between the control and the power circuit due to the large difference in voltages. Till date no on-chip capacitively coupled bootstrapping circuits was reported in literature, however such technique has already been employed using discrete components as in [85].

Same as for the first stage, all the control circuitry was implemented using analogue electronics to obtain a high efficiency since microprocessors, ADCs, DACs and clock generators all consume a substantial amount of power which may sometimes be higher than the power available from energy harvesters. Additionally, all the transistors in the control circuit operate in the sub-threshold region to limit the power dissipation in the transistors, thus further increasing the efficiency.

A higher conversion efficiency in the Buck converter is obtained by implementing synchronous switching, in which the freewheeling diode is paralleled with a switching device. Synchronous switching obtains a higher efficiency when the converter operates in Continuous Conduction Mode (CCM) but the efficiency is worse when the converter operates in DCM because the inductor current goes negative unless a zero current detector circuit is implemented [78]. In order not to implement a zero current detector circuit to avoid its power dissipation, an additional diode is required in the buck converter which although neutralises the

advantage of synchronous switching, it is still essential for the correct operation of the bootstrapping circuit when the converter operates in DCM.

The power conditioning circuit requires three identical buck converters. One is used to generate the output voltage as required by the load. Another one is required to generate the 1 V supply voltage for the MPPT control circuitry in the MPPT control. The third converter is employed to generate the 2 V supply voltage for the control circuitry of all three buck converters and the driving circuit part in the MPPT control. This means that one of the buck converters generates its own supply voltage and is responsible to cold start the whole power conditioning circuit. This can be achieved externally by connecting a capacitor between the regulators' input voltage and this converter's output. This converter's output needs to be connected to the regulators' control supply voltage and all the control circuits start up as soon as a voltage is present at the input.

3.3 Fabrication Technologies

A number of fabrication technologies available via a Europractice agreement were considered, mainly those offered by Austria Microsystems (AMS), Innovations for High Performance microelectronics (IHP), X-FAB and Taiwan Semiconductor Manufacturing Company (TSMC). The IHP high voltage option was not available and the TSMC's High Voltage (HV) option has a maximum working voltage of just 40 V. The X-FAB and AMS have a high voltage option of 45 V and 50 V respectively for their 0.35 µm technologies. Only X-FAB offers a high voltage option on the 0.18 µm technology. The most cost-effective, and verified solution at the time of fabrication of the first design was AMS. The XFAB 0.18 µm High Voltage (HV) technology is 50% more expensive than its 0.35 µm HV technology. Moreover, the AMS 0.35 µm HV technology is 40% cheaper than its X-FAB counterpart [86]. Since the switching frequencies in the power conditioning circuit are in the kHz range, its

implementation in 0.18 µm HV technology does not result in any improvement in efficiency. Moreover, since the 0.18 µm technology is a smaller technology than the 0.35 µm technology, the circuit suffers from higher leakage currents. The differences in mobility constants and threshold voltages of the transistors between all technologies is negligible. Hence it was decided that the most cost-effective technology for this circuit is the AMS 0.35 µm HV technology. The fabrication and packaging costs of this integrated circuit amounted to €6,590.

The second circuit was fabricated in December 2020 and its design started in January 2019. At the time AMS has informed all Universities that it intends to stop all Multi-Process Wafer (MPW) runs by 2020 and so AMS technology could not be used anymore by universities through the Europractice agreement. Therefore, it was decided to use a different technology for the second circuit to ensure that fabrication of the second circuit is possible. The second technology closest to the AMS in terms of process parameters is the X-FAB XH035 technology and so the second circuit is designed using this technology. The main disadvantages of X-FAB when compared to AMS is a breakdown voltage of 45 V instead of 50 V, a higher fabrication cost and lack of high voltage PMOS transistors with thin gate oxide layer. Furthermore shifting from one technology to another involves a learning curve to go through all the new Design Rule Check (DRC), process parameters and datasheets of the primitive devices for the new technology [84]. Various circuit blocks such as the comparator and the Schmitt inverter which could have been reused for the second circuit had to be redesigned. Eventually AMS continued to offer MPW runs for high voltage technologies until 2021 but by then the second design was already in the layout stage and it was not possible to go back to AMS technology given that the design was at an advanced stage. The novelty of the circuit designs and architectures is not affected by the technology being used.

3.4 Conclusion

This chapter highlighted the novel aspects of the proposed power conditioning circuit and presented a preliminary study, based on system level simulations, which were carried out to verify the feasibility of the proposed architecture. In addition, this chapter also discussed the considerations related to the fabrication technology used for this circuit. The next chapter describes in detail the design of all the circuit blocks to implement the AC/DC-to-DC converter with MPPT function, which is the first stage of the proposed power conditioning circuit.

4. AC/DC-to-DC Converter with MPPT Control Circuit

4.1 Design of Proposed AC/DC-to-DC Converter with MPPT Control

The research presented in this dissertation, initially focused on the design of the first stage of the proposed power conditioning circuit (refer to Figure 3.1), which is the AC/DC-to-DC converter together with its MPPT and control circuit. Preliminary simulations carried out, resulted that a Perturbation and Observation (PO) algorithm is more stable for this application. However, both the PO algorithm and the Incremental Conductance algorithm were still designed and simulated in Cadence.

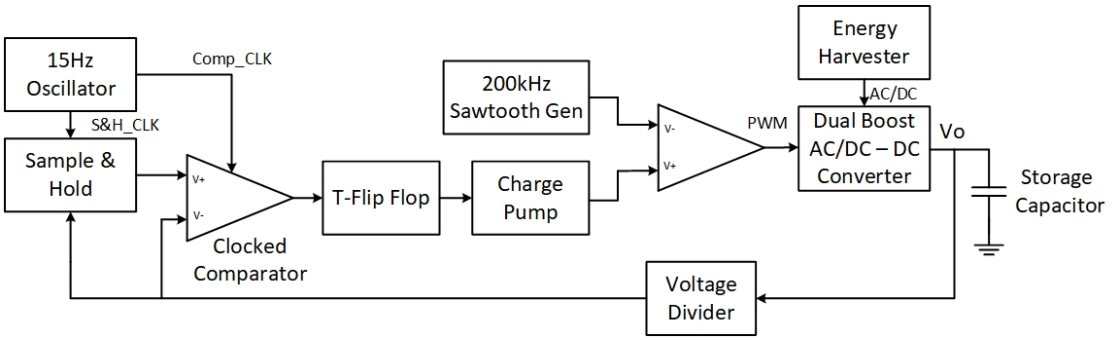

Figure 4.1: Block diagram of the proposed Perturbation and Observation MPPT AC/DC-to-DC Converter.

The full block diagram of the AC/DC-to-DC Converter with PO MPPT algorithm is represented in Figure 4.1. Part of the control circuit of the power conditioning circuit requires a 2 V voltage supply while another part requires a 1 V voltage supply. These are generated via the voltage regulating DC-DC converter as shown in Figure 3.1. All the control circuitry (even those having a 2 V supply) is able to work with a supply voltage of 1 V. Thus, as the energy harvester generates a minimum voltage of 1 V, this voltage forward biases the diodes in the AC/DC-to-DC converter and charges the storage capacitor to this voltage. At this point, the regulators in the voltage regulating DC-DC Converter supply 1 V to both the 1 V and 2 V supplies which is enough for the converter to initiate its operation from cold start. This ensures minimal power loss from the energy harvester when the converter is required to cold start. In addition, since the control stage operates at such a low voltage, minimal power is dissipated by the control circuit itself. The circuits requiring a 2 V supply are the comparators and the PWM generation comparator circuit. This is because the differential inputs of the comparators must work at the full voltage range required from 0 V to 1 V. In addition, for the power transistors in the AC/DC-to-DC Dual boost converter to operate with minimum conduction losses, the PWM generation comparator circuit applies a voltage of 2 V to their gate terminals and hence the gate drive circuit requires a 2V supply voltage. These transistors can work with a gate voltage of 1 V which means that the converter is still able to start boosting the voltage as soon as the power conditioner cold starts at an input voltage of 1 V. Once the converter starts boosting the voltage, and generates a voltage of 2 V, then the converter starts operating at its maximum efficiency as the gate voltage applied would now be 2 V.

The first stage in the schematic diagram is the oscillator. This generates the required clock pulses for the Sample and Hold (SH) circuit in the Perturbation and Observation MPPT. The SH circuit then charges its internal capacitor to the

output voltage via a transmission gate which requires both the clock signal and the inverted clocked signal as supplied by the oscillator. Once enough time is allowed for the SH capacitor to charge to its expected voltage, the oscillator switches off the transmission gate and waits for some time so that the converter's operation is allowed to respond to the changing duty cycle. Then the oscillator switches on the clocked comparator. The aim of having a clocked comparator purpose is to compare the voltage stored in the internal capacitor of the SH to the actual voltage coming from the converter's output. If the actual voltage is higher, then the output of the comparator would remain zero but if the actual voltage is lower, then this means that the converter's output voltage is dropping. Hence the comparator's output would go high to change the state of the TFF which is the subsequent circuit in the schematic diagram. In this implementation, the output from the SH circuit is connected to the non-inverting input of the comparator while the actual output voltage is connected to the inverting input of the comparator. The comparator is clocked so that the control circuit allows the converter to react to the changing duty cycle between clock pulses.

The T-flip flop changes state every time the comparator detects the output voltage of the converter dropping. The T-Flip Flop's output then drives a charge pump which consists of a current starved half bridge either charging or discharging a capacitor at a very low current. According to the T-Flip Flop's state, either the pull-up transistor or the pull-down transistor switches so that the voltage of the capacitor increases or decreases accordingly. This gradually changes the duty cycle at which the converter's power transistors are operated. In order to generate the PWM with the duty cycle depending on the voltage stored in the charge pump's capacitor, another comparator was required. The non-inverting input of the comparator is connected to the output's charge pump while the inverting input is connected to the sawtooth generator. The frequency of the sawtooth generator determines the switching frequency of the power transistors

inside the dual boost converter. The optimized switching frequency was set at 200 kHz (refer to Chapter 3). Since most of the time, the converter's operation is in DCM a high switching frequency is beneficial to enable more power transfer through the converter. However, a compromise had to be reached since high switching frequencies would mean more power dissipation due to the gate charging and discharging in the power transistors and higher switching losses in the power transistors and diodes of the converter. The comparator's output then drives the gate driver, which is a half bridge inverter, to charge and discharge the gate capacitance of the power transistors. The subsequent circuit block is the dual boost converter. In order to close the loop, the output voltage is fed back to the SH circuit and the comparator. The converter was designed to generate a voltage of up to 50 V whereas the operating voltage of the control is just 1 V. Supplying a voltage which can reach up to 50 V to the control is not possible and therefore, this had to be lowered to a maximum voltage of 1 V. That is the scope of the voltage divider block which reduces the voltage by a ratio of 1:50.

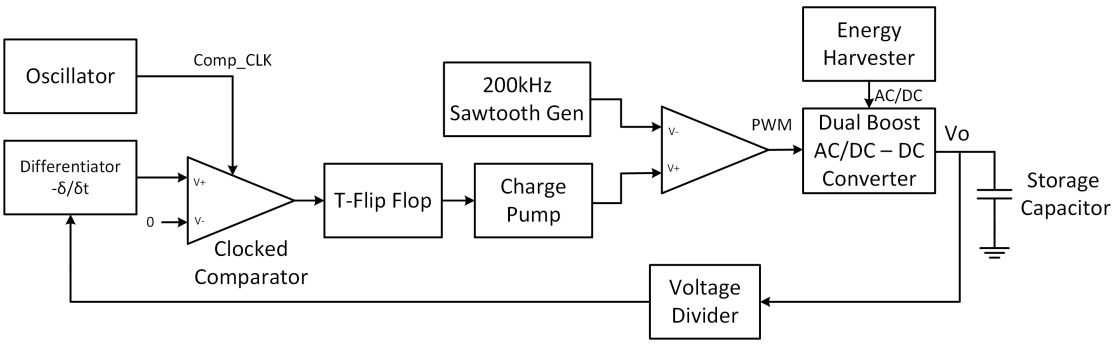

Figure 4.2: Full block diagram of the proposed Incremental Conductance MPPT AC / DC –DC Converter

The full block diagram of the AC / DC–DC Converter with Incremental Conductance MPPT algorithm is represented in Figure 4.2. The main differences in this circuit when compared to the PO approach is that the SH circuit is replaced by a differentiator and the clocked comparator compares the differentiator output

with 0 V. Another minor difference is that a low frequency oscillator was required to generate 20 Hz pulses rather than 15 Hz as deduced from the PLECS simulations reported in Section 3.1.2. Also the oscillator generates a clock pulse for the comparator only.

4.1.1 Low Frequency Clock Generator

The first block in the schematic diagram is the oscillator which supplies the clock pulses to the SH circuit and the clocked comparator and was designed to generate a clock frequency of 15 Hz when implemented in the PO MPPT algorithm. The same circuit with some minor optimisation was designed to generate a frequency of 20 Hz when implemented in the Incremental Conductance MPPT algorithm. In the second implementation, the oscillator had to supply the clock pulses to the Differentiator amplifier and to the clocked comparator. These two clock frequencies were found to operate each MPPT reliably, as confirmed from the simulations carried out in PLECS reported in Section 3.1.2. The oscillator generates both the clock pulses and the inverted clock pulses as required by the clocked circuits.

In order to design an on-chip oscillator with such a low frequency, a literature review on the state-of-the-art of such oscillators was carried out. The types of oscillators studied were resonant LC oscillator, ring oscillator, wave oscillator, and negative resistance differential oscillator. The Colpitts and Hartley LC oscillators, and the negative resistance differential oscillator require a very large capacitor and a very large resistor or inductor in order to get the low frequency required. These components would take up a very large area on the chip being designed. No oscillators could be found that can generate such a low frequency unless using substantial area on the chip being designed. The conventional CMOS ring oscillator generates a frequency in the order of MHz [87, 88]. In order to produce a lower frequency signal of the order of hundreds of Hz, the ring oscillator would require thousands of inverter gates to reach the propagation delay for the

frequency required which is also impractical. Although this approach is capable to accurately generate its designated frequency, its main drawback is the high power consumption. Alternative circuit topologies, such as relaxation oscillators, exist but they are not capable of generating low frequency signals unless very large off-chip passive components are used [89].

An ultra-low frequency ring oscillator using the concept of CMOS thyristors, was designed in [90]. The main drawbacks of this oscillator are that it requires a minimum supply voltage of 2.5 V, occupies a considerable area since it requires three capacitors and dissipates a static power of 5.7 µW.

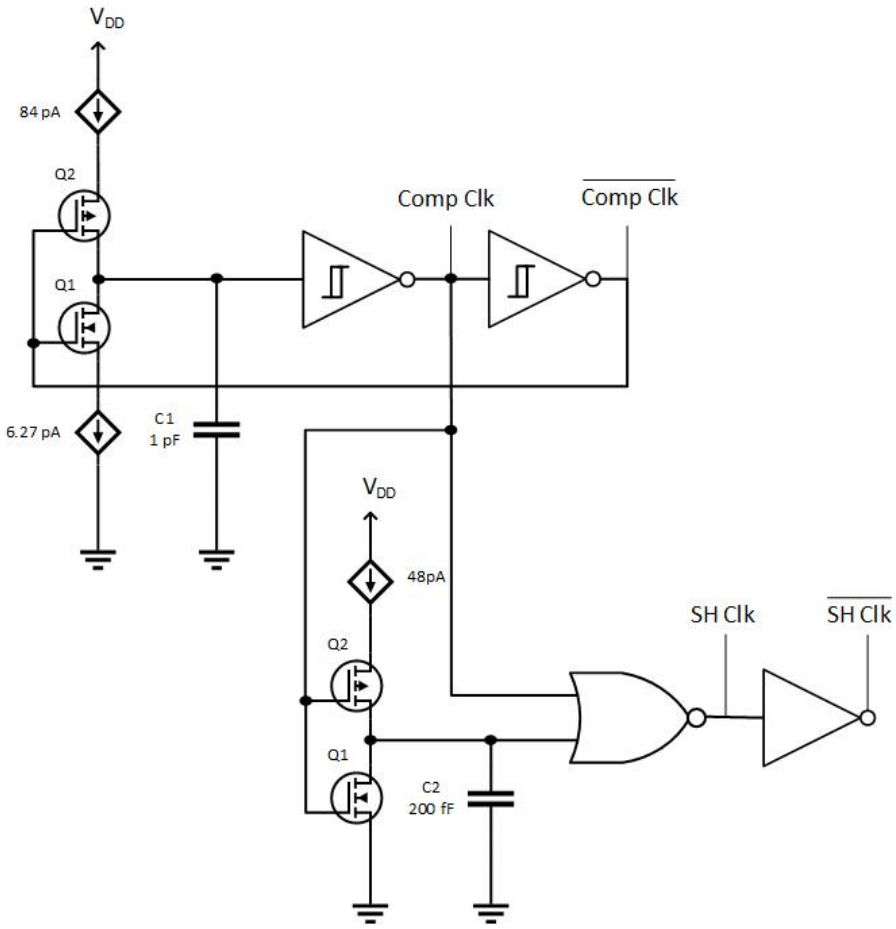

Figure 4.3: Oscillator simplified circuit diagram

The low frequency oscillator proposed in this work is achieved by looping two Schmitt inverters with a current starved inverter as shown in Figure 4.3 [13]. The current starved inverter charges and discharges an on-chip timing capacitor of 1 pF which uses up to 1149 µm^2. The charge pump current charging and discharging this capacitor is controlled via two current mirrors from a reference current. In the preliminary design, the third inverter was implemented by a normal inverter gate rather than a Schmitt inverter. However, the oscillator did not operate correctly because simulations has shown that the inverter was changing its state before the previous Schmitt inverter reaches 1 V and so the current starved inverter starts the discharging process of the timing capacitor prematurely with the comparator clock never reaching 1 V. Hence for this reason, the third inverter had to be implemented by another Schmitt inverter. Although this approach led to a higher area consumption, it meant that the oscillator operates with lower losses because a Schmitt inverter quenches the leakage currents thus resulting in lower static power losses [91] apart from improving the noise immunity of the oscillator [92].

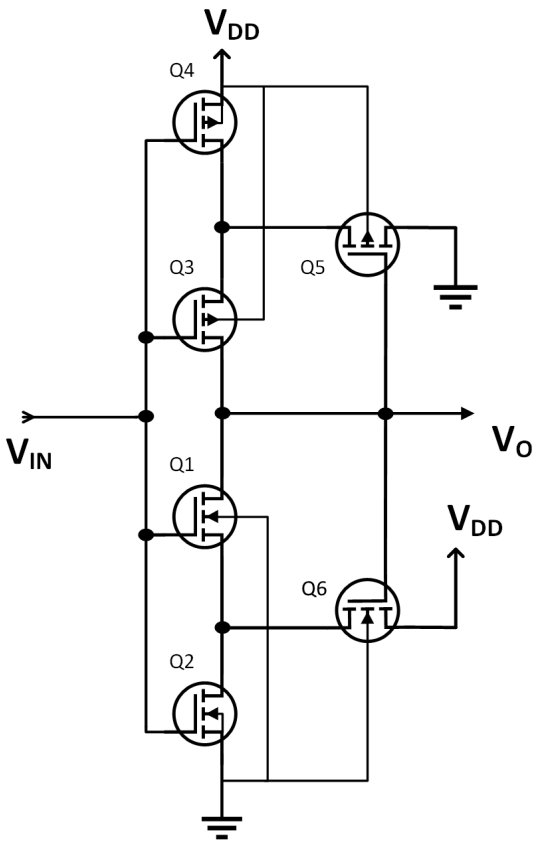

Figure 4.4: Schmitt Inverter Circuit Diagram [91]

Transistor Name	**Width**	**Length**
Q2	0.4 µm	5 µm
Q4	0.4 µm	1 µm
Q5	5 µm	0.35 µm
Q6	5 µm	0.35 µm

Table 4.1: Transistor sizes of the Schmitt Inverter

The Schmitt inverter, shown in Figure 4.4, uses four stacked transistors to invert the input signal and two additional transistors, *Q5* and *Q6*, to feedback the output voltage [91] [93] and alter the threshold voltage of the inverter depending on the current state of the inverter [13]. The transistor sizes of the Schmitt inverter are

listed in Table 4.1.

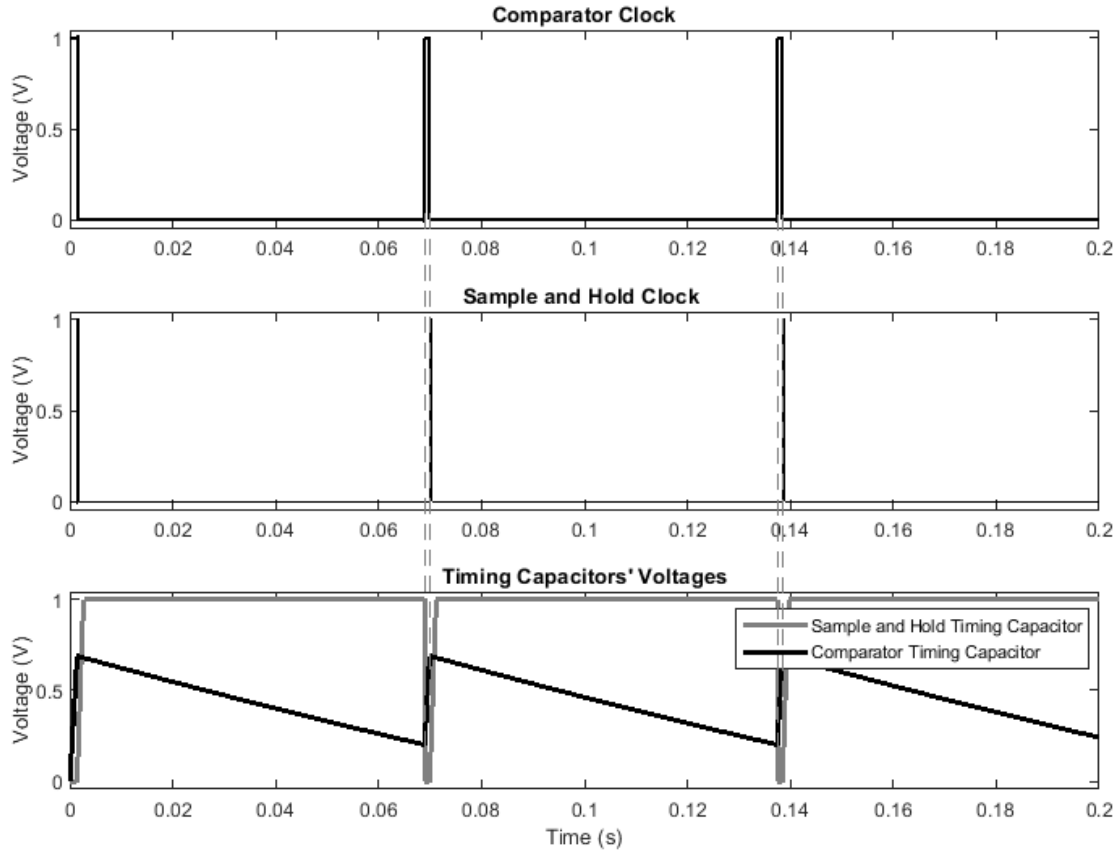

Figure 4.5: 15 Hz oscillator simulation results of the two-timing capacitor voltages, comparator, and sample and hold clock pulses.

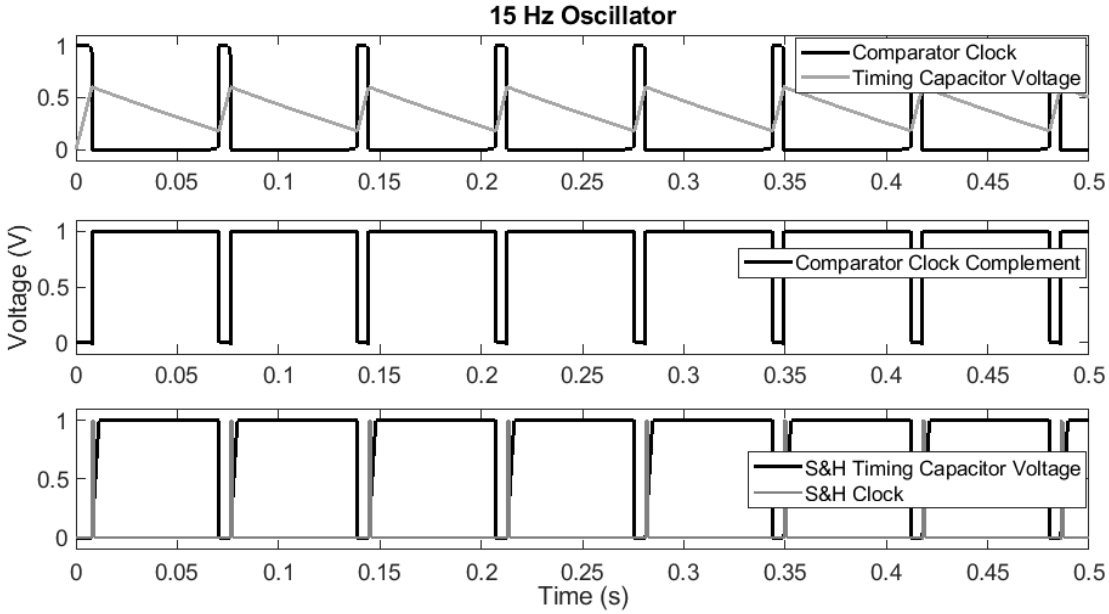

Figure 4.6: Transient simulation results of the 15 Hz oscillator showing the clock pulses fed to the comparator and the sample and hold circuits.

The current employed in the current starved inverter, the capacitance of the capacitor and the hysteresis values of the Schmitt inverter determine the clock frequency and the duty cycle of the clock pulses shown in Figure 4.5. Both the pull up transistor and the pull-down transistor being driven via the current mirror required a reference current circuit. This circuit was designed, and it generates a reference current of 1.6 nA. Its design is explained further on in Section 4.1.2. Figure 4.6, shows the voltage of the timing capacitors. The charging time of the timing capacitor determines the clock pulse width. On the other hand, the discharging time of the timing capacitor determines the time between each clock pulse. The oscillator's frequency is determined by these two timings. While the required clock frequency is ultra-low, high precision was not essential in this design.

In fact, the requirements of this oscillator are ultra-low frequency and very low power consumption which can only be achieved by very low currents. Therefore, all transistors are operated in the sub-threshold region. Transistors operating in

this region are more susceptible to process and temperature variations and so simulations on this oscillator, taking in consideration these variations were carried out. The clock pulses to be supplied to the clocked comparator should be wide enough for the comparator to compare the current output voltage with the previous output voltage stored in the SH circuit, apply a corresponding output to the TFF and allow enough time for the TFF to change its state. The comparator was also designed with low bias currents for minimal power consumption and so its slew rate is limited. Moreover, the internal timing capacitor is not allowed to charge too rapidly so that it would not lead to a voltage dip in the voltage supply which may cause glitches in the rest of the control circuitry. Hence a 2 ms clock pulse width was targeted, which is equivalent to 3 % of the time period. However, in order to give allowance due to temperature and fabrication conditions, the target at typical conditions was increased to 10 % or 7 ms. The targeted hysteresis limits of the Schmitt inverter are from 190 mV to 590 mV. Hence the charging current required was calculated as follows;

$$I = C\frac{\delta V}{\delta t} = 1pF \times \frac{400mV}{7ms} = 57pA \tag{4.1}$$

On the other hand, the discharging current required was calculated as follows;

$$I = C\frac{\delta V}{\delta t} = 1pF \times \frac{400mV}{60ms} = 6.67pA \tag{4.2}$$

The transistors in the current mirror are sized accordingly to obtain these currents. A leakage current of 0.5 pA/µm was taken in consideration [94]. The 1.6 nA reference current was scaled down for the charging current mirror using Eq. 4.3;

$$I_{D1} = I_{D2}\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \tag{4.3}$$

Transistors Q1 and Q2, which either charge or discharge the timing capacitor depending on the oscillator's output, were kept as minimum size transistors.

This 15 Hz oscillator also generates the clock pulses to the SH circuit to store the voltage across the storage capacitor for the next comparator clock cycle. This clock pulse, labelled SH_Clk in Figure 4.1, is fed to the transmission gate of the SH circuit shown in Figure 4.11 and goes high exactly once the comparator's clock pulse is over. This clock pulse should be wide just enough for the sample and hold's capacitor to reach the input voltage but not too wide in order to leave enough time for the converter to react to the changes in duty cycle until the next comparator clock cycle. It was found that a clock pulse with a width of about 10 µs would be enough for the SH to store the required value.

When the Comp_Clk is at 1 V, the 200 fF capacitor is discharged through transistor Q1 and so the output of the NOR gate being the SH clock is at logic zero. As soon as the Comp_Clk is 0 V, the NOR gate output goes to 1 V which initiates the SH clock pulse. Consequently, the 200 fF capacitor initiates the charging process via a current mirror from the same reference current circuit of the oscillator. Once it charges to 340 mV which is considered a high state by the gate, the NOR gate output goes back to 0 V and the SH clock pulse is over.

The Schmitt inverter shown in Figure 4.4, uses four stacked transistors to invert the input signal [91] and two additional transistors, Q5 and Q6 feedback the output voltage. Such Schmitt inverter is commonly used instead of standard inverters to effectively quench its leakage current [91] and provide a better noise immunity together with a noise stable operation especially in low voltage and low power applications [93]. By feeding back the output voltage through transistors Q5 and Q6, the threshold voltage of the inverter is altered depending on the current state of the inverter, as to be explained. When the input is increasing from low state to high state, transistor Q2 switches on once its threshold voltage is exceeded and transistor

Q6 is already switched on since the output of the inverter is high. Hence the source voltage of transistor Q1 is effectively a voltage divider between the on-resistances of transistors Q2 and Q6. For the inverter to change its state, the input voltage should reach the sum of the source voltage and the threshold voltage of transistor Q1. In order to increase further the input high state voltage, both the channel width of transistor Q6 and the channel length of transistor Q2 were increased to 2 µm. In addition, to further decrease the lower triggering voltage, the channel width of transistor Q5 was increased to 5 µm, however the channel length of transistor Q4 could not be increased because the inverter ended not being able to change its output state to 1 V at all the temperature conditions tested especially in the worst speed corner analysis at a temperature below 0 °C. When the input voltage is increasing from 0 V to 1 V, the drain to source resistance R_{DS} of transistors Q2 and Q6 was estimated to be 122 MΩ and 1.01 MΩ respectively, just before the output changes state. These values were calculated from g_{ds}. Although transistor Q2 operates in the active region, transistor Q6 falls in the sub-threshold region since it maintains its source voltage at the highest voltage possible until it switches off because in the process its gate to source voltage drops.

Throughout its design, the oscillator was continuously tested at various temperature conditions and also corner analysis in order to obtain a robust design which is less susceptible to such fabrication and environmental changes. The optimised design and its power dissipation (including reference current circuit) are listed in Table 4.2. Since the most important aspect of this whole circuit is efficiency, one could not opt to high precision oscillators because they would require higher currents to operate correctly and will eventually consume more energy. Hence continuous simulations were carried out to ensure that the operation of the oscillator does not alter substantially. Although the 15 Hz oscillator frequency is the ideal frequency for the MPPT circuit, small variations to this frequency would not jeopardise its correct operation. Corner analysis and Monte Carlo simulations

were carried out to obtain a robust design. The frequency may drift from 10 Hz to 22 Hz when simulating with both temperature and process variations. Monte Carlo simulations resulted in a standard deviation of 6 Hz. The offset variation of the oscillator output frequency from the nominal 15 Hz are not expected to affect the operation of the MPPT circuit. Table 4.3 compares the performance of the proposed oscillator with the state of the art (SOA). The temperature coefficient and voltage coefficient of the oscillator's output frequency are 0.27 %/°C and −0.069 %/mV respectively. The area usage of this oscillator including the 200 fF capacitor required to generate the SH clock pulse is of 1645 µm^2.

Model Libraries	**Temp.** (°C)	**Frequency (Hz)**	**Comp. Pulse (ms)**	**SH Pulse (ms)**	**Cons. (nW)**
Typical	0	16	7.95	1.5	15
	27	15	6.3	1.2	30
	80	16	5.5	0.8	90
Worst Speed	0	22	2.74	1.0	2.0
	27	17	3.8	0.8	2.5
	80	13	2.55	0.7	9.3
Worst Power	0	10	16	2.1	161
	27	10	14	2.2	279
	80	14	10.9	3.1	552

Table 4.2: 15 Hz oscillator performance in schematic simulations at different temperature and fabrication conditions

Reference	**Technology**	**Min. Supply Voltage (V)**	**Frequency (Hz)**	**Power (nW)**
[95]	180 nm CMOS	2.5	0.303	6.6
[90]	250 nm CMOS	2.5	8.94	5700
[96]	2 µm CMOS	2	100	300
This Work	0.35 µm CMOS	1	15	30

Table 4.3: Comparison of the 15 Hz oscillator with the State of the Art

4.1.2 Self-Biased Current Reference Circuit

A self-biased circuit generating a reference current which is both temperature and supply voltage independent was required. Although several temperature and voltage independent current reference circuits exist, they usually generate a reference current in the µA range or higher.

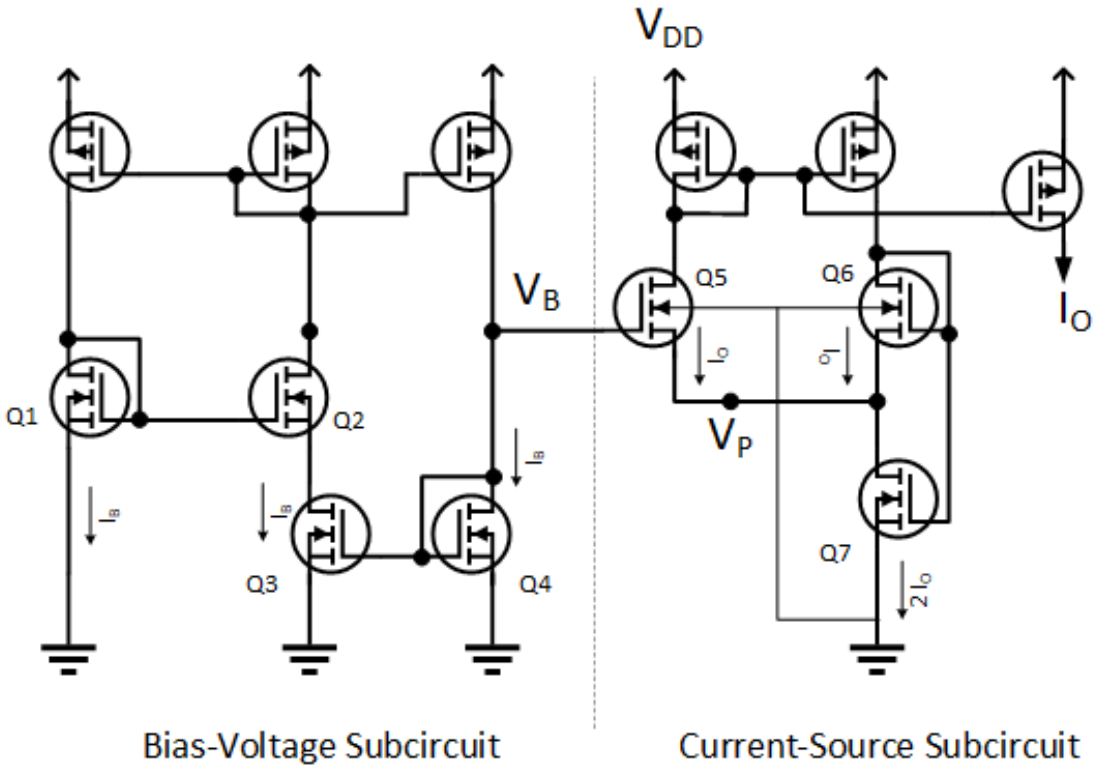

Figure 4.7: Temperature and Supply Voltage Independent Current Reference Circuit designed using CMOS MOSFETs operating in the subthreshold region [97]

A reference current circuit shown in Figure 4.7, generates a temperature and supply voltage independent reference current of 95 nA [97]. This circuit was designed using CMOS MOSFETs operating in the subthreshold region so that minimum power is dissipated by this circuit. However, according to the reported practical results, this circuit still consumes a power of 1 µW. The target overall power consumption of the whole control circuit of the power conditioner is around 1 µW and therefore a lower power consuming current reference circuit is required. This circuit was modified and improved for lower power consumption. The newly designed circuit is shown in Figure 4.8 and the transistor sizes listed in Table 4.4.

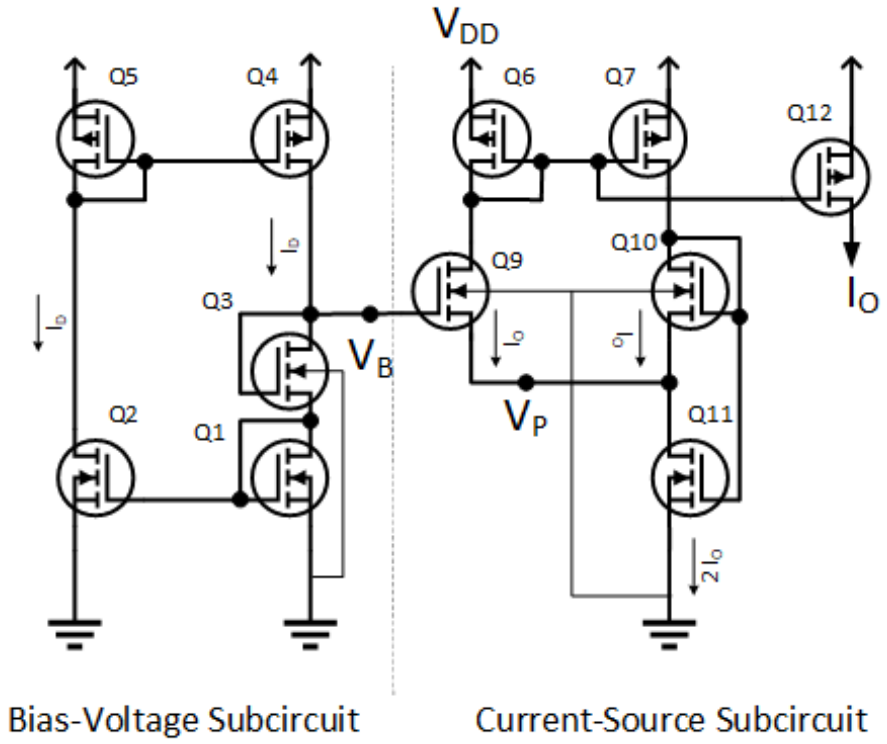

Figure 4.8: Self-biased temperature and supply voltage independent current reference circuit using CMOS MOSFETs operating in the subthreshold region modified for lower power consumption

Transistor Name	**Width**	**Length**
Q1	10 µm	0.35 µm
Q3	5 µm	0.35 µm
Q9	0.4 µm	20 µm
Q10	0.5 µm	1 µm
Q11	10 µm	0.35 µm

Table 4.4: Transistor sizes of current reference circuit

This circuit consists of a self-biased voltage reference sub-circuit which generates a voltage V_B. This voltage then biases the current-source sub-circuit to generate an output current I_O. The former exhibits a positive temperature coefficient,

whereas the current source sub-circuit exhibits a negative temperature coefficient. If sized correctly, a resultant zero net temperature coefficient output current can be obtained.

The bias-voltage sub-circuit was redesigned to require only a self-biased Wilson current mirror [98] and this resulted in one less current path in the bias-voltage sub-circuit. In order to reach the required bias voltage for *Q9* with lower currents, the diode connected transistor *Q3* was added. The modified circuit was analysed in Appendix A. The transistor body effect was not taken in consideration in the derivations because it does not affect the thermal stability of the circuit.

Equation (A.48) proves that the modified current reference circuit is independent of temperature variations. Furthermore, it can be deduced that the thermal coefficient of the output current can be minimised through appropriate adjustment of the threshold voltages of *Q1, Q3, Q9, Q10* and *Q11*. This can be achieved by appropriate sizing. The reference current circuit designed for the oscillator consumes a power of 7.6 nW at a temperature of 27 °C. The current output variation with temperature is presented in Fig. 4.9.

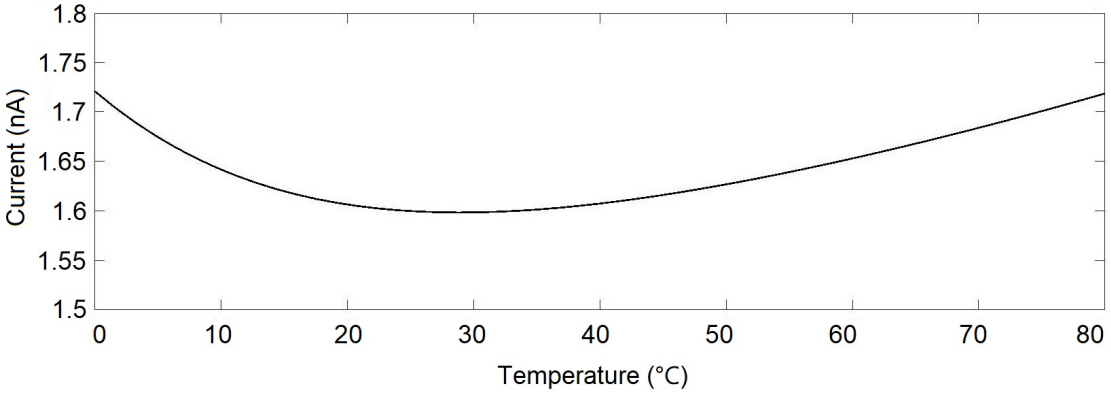

Figure 4.9: Variation of the current reference output with temperature

4.1.3 Differentiator Operational Transconductance Amplifier

A low power Operational Transconductance Amplifier (OTA) requiring a bias current of 30 nA at the differential stage and 90 nA at the output stage was designed. This OTA consumes a total power of 125 nW. A compensation capacitor C2 was also included to increase the stability of the OTA. This OTA was then used as a differentiator amplifier. However, when the differential amplifier was designed and simulated in Cadence, it did not work as expected and hence the circuit had to be improved further. The first challenge was that the OTA ideally should have a dual rail supply but this would eventually require an additional switching converter to generate a negative supply. Hence as a work around, the inputs of the OTA were offset by 100 mV. This was achieved by applying a voltage of 100 mV at the non-inverting input instead of connecting it directly to ground as conventionally done in differentiator amplifiers. Another problem is that the change of the output voltage occurs at a very slow rate and this gradient is decreased even further by a factor of 50 by the voltage divider block. Hence the differentiator does not generate a differentiated voltage which is large enough to be detectable by the comparator in the next stage. Consequently, the noise was larger than the differentiated voltage and hence as a solution, it was decided that the input of the differentiator is passed through a clocked transmission gate. This was done so that the change is inputted abruptly at every clock cycle, thus generating a higher differentiated output. Clock feedthrough generated by the transmission gate was insignificant and no noticeable issues were recorded in the simulation of the operation of the circuit, since the transmission gate transistors are small and the magnitude of the clock pulses is limited to only 1 V.

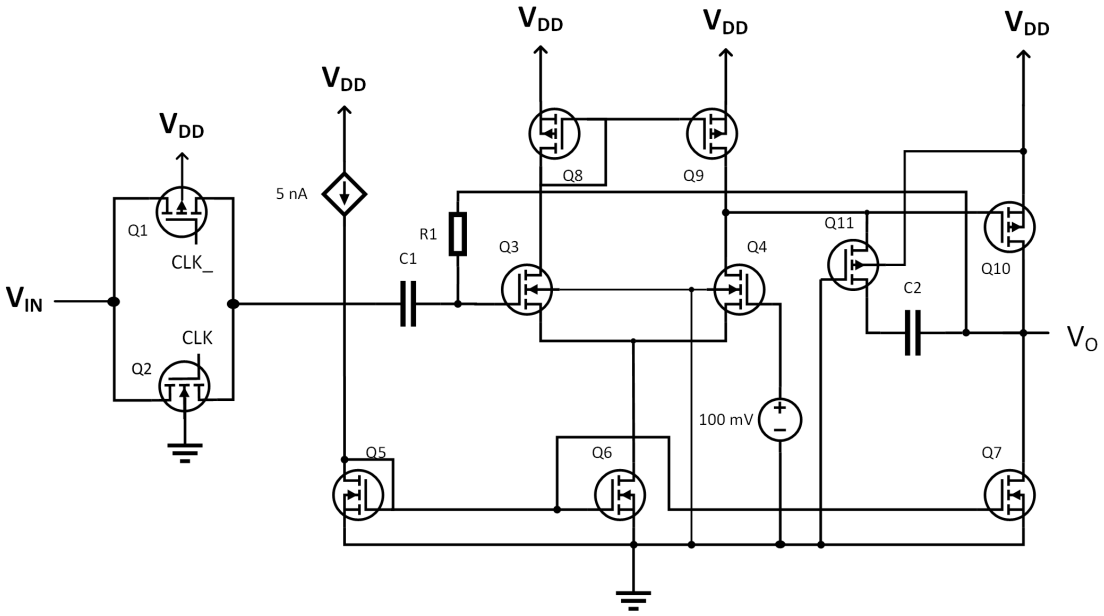

Figure 4.10: Design of a very low current bias operational amplifier to implement a differentiator with a clocked input.

The final circuit is shown in Figure 4.10. R1 and C1 are 10 kΩ and 2 pF respectively and these were intended to be integrated even though they would consume a substantial amount of chip area. Although these two mitigations improved the operation of the Incremental conductance MPPT, the sensitivity of the differentiator was worse when compared to the PO circuit. Therefore, since the PLECS simulations concluded that the PO algorithm is the most efficient algorithm for this application, and when considering the challenges encountered to design a differential amplifier with such a low change in output voltage, it was decided that the way forward was to focus on implementing only the PO algorithm.

4.1.4 Sampling and Hold Circuit

The Sampling and Hold circuit shown in Figure 4.11 is a simple circuit intended to store a particular voltage into a capacitor. During the sampling, a transmission gate consisting of a PMOS and an NMOS transistors which are connected in parallel

are switched on in order for the input voltage to be fed in the storing capacitor. On one side the capacitor needs to be as small as possible to minimise the charging time and not affect the voltage being sampled. On the other hand the capacitor needs to be large enough for the voltage being stored not to be discharged through current leakages thus the voltage being stored is altered substantially.

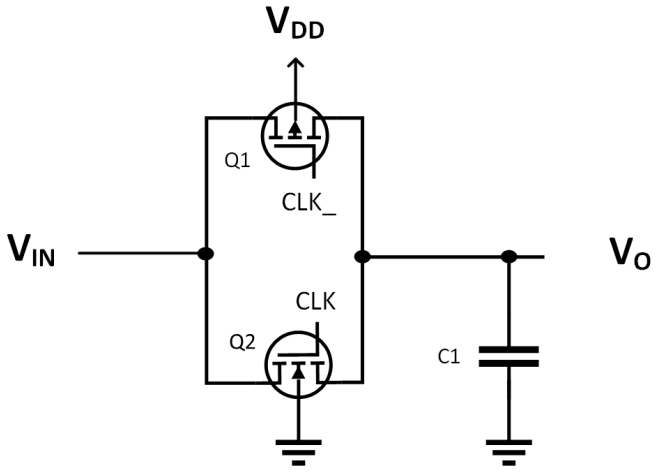

Figure 4.11: Sampling and Hold Circuit

Capacitor C1 is sized 200 fF while the transistor sizing of the transmission gate was optimised in order for the capacitor to be able to charge to 1V and discharge to 0V during the clock pulse width of 0.7 ms which is the minimum clock pulse which can be generated by the oscillator due to fabrication and environmental conditions. The channel width of the NMOS transistor was set to 0.5 µm and the channel width of the PMOS transistor was set to 10 µm. In certain simulations, transistor Q1 failed to fully charge capacitor C1 to V_{IN} in a clock period of 0.7 ms. Hence transistor Q1 was sized to be substantially larger than transistor Q2 to ensure charging capacitor C1 to V_{IN} in 0.7 ms. No issues were detected in simulations with the discharging of capacitor C1 to V_{IN} through transistor Q2.

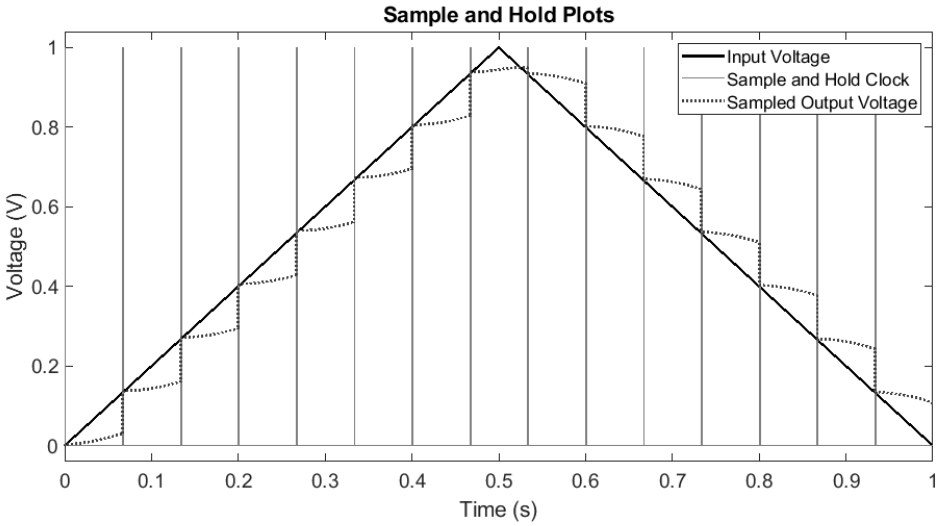

Figure 4.12: Transient simulation of the Sample and Hold circuit clocked at 15 Hz with a voltage sweep applied to its input.

Figure 4.12 shows the plot obtained when simulating the SH input voltage, output voltage and the clock fed from the 15 Hz oscillator. This simulates the SH circuit with an input voltage changing at a rate of 2 V/s. No clock feed through and charge injection is seen in the simulations due to capacitor C1 in the SH circuit. Some leakage is present from the input side towards the output side during the hold period mainly due to the low clock frequency at which the SH circuit is operated and the low value of the capacitor storing the voltage. This issue could be mitigated by further increasing the capacitor value, but this would lead to a larger area usage and larger transistors in the transmission gate. However, in practice, it is expected that the leakage is much less mainly because the change in voltage will be much lower than the simulated 2 V/s. A more realistic value of the rate of voltage change at the input of the SH circuit is 0.2 V/s. The SH circuit dissipates an average power of 5.66 fW.

4.1.5 Clocked Latched Comparator

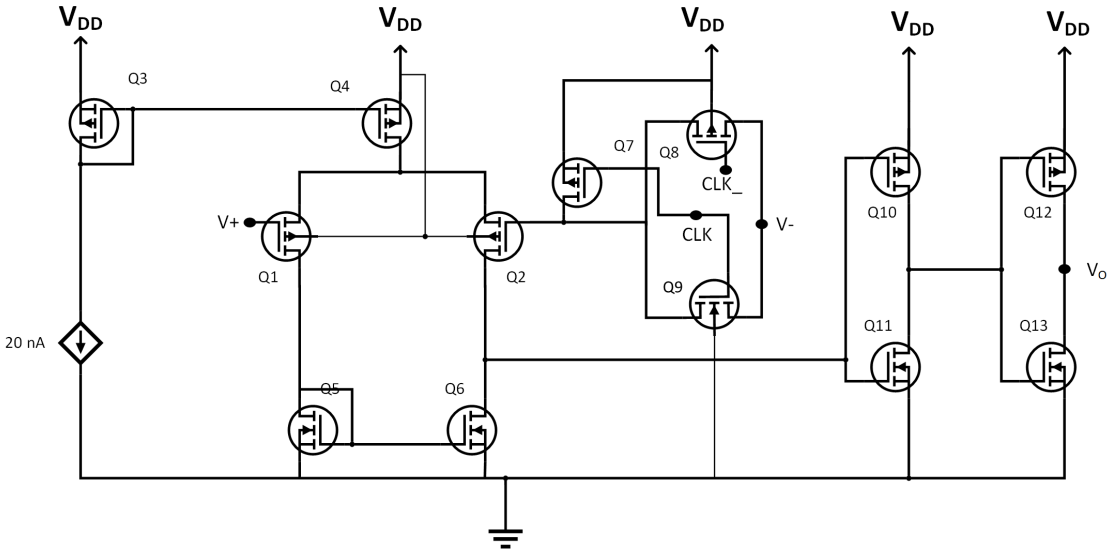

Figure 4.13: Clocked Comparator Circuit Diagram

The clocked comparator circuit is shown in Figure 4.13. The control circuit is designed to operate at a supply voltage of 1 V. This enabled the power conditioning circuit to be able to cold start at a low voltage thus maximising the harvested energy. Operating at such a low voltage made the design of operational amplifiers and comparators more challenging because their inputs and output had to be able to work from rail to rail, that is between 0 V and 1 V. Also, their correct operation had to be ensured even when the inverting input and non-inverting input were close to the rail voltages. In order to ensure correct operation of the comparators when the inverting and non-inverting inputs are close to 0 V, the comparator design made use of a PMOS differential circuit and to work with input voltages close to 1 V, it was decided that the circuit should be supplied with a 2 V supply since this was already available from the PWM generation comparator circuit supply voltage. The 2 V supply would be generated as soon as the converter cold starts once a minimum input voltage of 1 V is generated by the energy harvester. The comparator starts working with a 1 V supply voltage and once the converter starts

boosting the voltage, the comparator's supply voltage would go to 2 V and hence at this point, it operates at the full voltage range as required. There is no risk that the comparator's inputs will be close to 1 V because the voltage across the output storage capacitor is at 1 V just as the circuit has cold started and the voltage divider which drives the inverting input of the comparator, factors it down to 20 mV. The comparator is clocked so that enough time is allowed for the converter's output to settle to the changes in the duty cycle until the actual voltage is compared to the voltage stored in the Sample and Hold. The comparator's output was turned off by blocking the voltage to the inverting terminal via a transmission gate and applying a high voltage to its gate thus switching off the differential circuit. The power consumption of the comparator was a priority in design stage. Since the comparator is clocked at 15 Hz with a clock pulse of more than 2 ms, the slew rate is not an issue and hence the bias currents could be set as low as possible to guarantee a low power dissipation. A 20 nA bias current was enough for the comparator's correct operation in which the transistors were operated in the sub-threshold region. All transistors in the differential circuit were matched and their sizing was set to achieve a sensitivity of 2 mV between the inverting and non-inverting terminal.

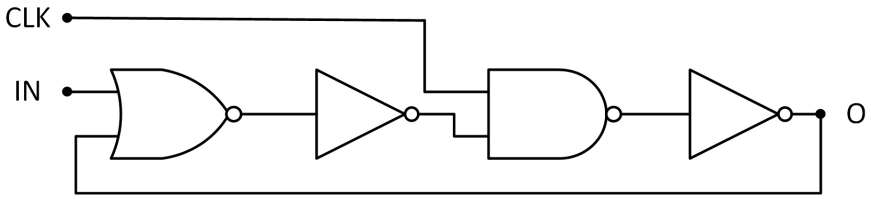

Figure 4.14: Comparator Output Latch

During simulations, an issue with the design emerged. The inverting terminal signal is connected to the output of the voltage divider which includes the output voltage ripple due to the switching of the AC/DC-to-DC converter. Hence when the inverting and non-inverting terminals of the comparator are quite close, the output of the comparator kept fluctuating between high and low levels. This posed

a serious issue because the TFF's output kept oscillating.

In order to eliminate this issue, the output of the comparator was modified so that its output is latches to the clock signal. A cross-coupled transistor latch could have been employed but such latch tends to be sensitive to the slew rate of the previous circuit which varies depending on the fabrication and temperature conditions of the circuit. Therefore, for simplicity and reliability purposes, a digital circuit having four gates was implemented. This was achieved as shown in Figure 4.14. The required Boolean expression was derived and simplified using Karnaugh maps. The expression obtained is $O = Clk.(In + O_{-1})$. These additional gates ensured that no fluctuation and ringing is generated at the output of the clocked comparator due to the ripple voltages generated at the converter's output. As shown in Table 4.5, whenever the Clock signal and the output of the comparator go high, the output of the latch would remain high until the clock pulse goes back to low state.

$\mathbf{O_{-1}}$	**IN**	**CLK**	**O**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 4.5: Truth Table of Clocked Comparator Output Latch

The gates were designed from transistor level. The static power consumption of the designed gates is in the pA range. These gates switch at a very low frequency and so the source of the power dissipation is more attributed to the comparators'

and oscillators' current mirrors and the converter's efficiency.

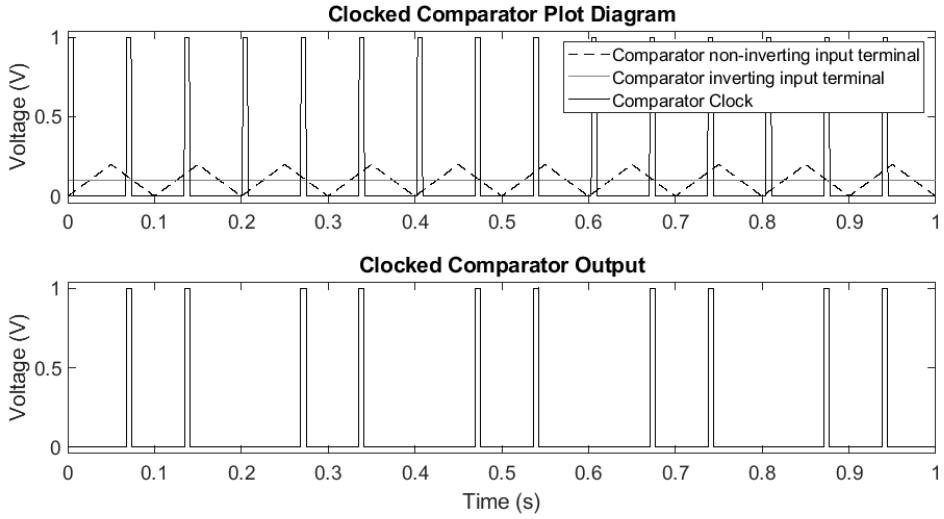

Figure 4.15: Transient simulation results of the clocked Comparator operating at a clock frequency of 15 Hz, 100 mV applied to the inverting terminal and triangular wave applied to the non-inverting terminal.

A standalone simulation of the clocked comparator block was carried out, and the results are shown in Figure 4.15. The clocked comparator dissipates an average power of 12.3 nW throughout its operation.

4.1.6 Toggle Flip - Flop

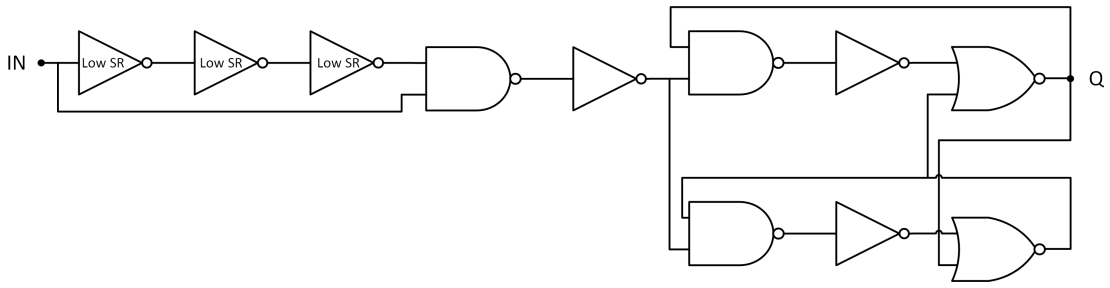

Figure 4.16: Toggle Flip Flop Schematic Diagram

The TFF circuit diagram is shown in Figure 4.16. This circuit consists of a positive edge trigger and an asynchronous TFF. It is designed following a derivation carried

out by using De Morgan's law.

$$Q(t+1) = \overline{IQ(t) + \overline{Q(t)}} \tag{4.4}$$

$$\overline{Q(t+1)} = \overline{I\overline{Q(t)} + Q(t)} \tag{4.5}$$

The TFF is supposed to change its state at every clock pulse applied by the clocked comparator so that the maximum power point of the energy harvester is continuously sought. In order to get enough propagation delay in the positive edge trigger and generate a pulse long enough for the TFF to change state, three low speed inverters are used. The flip flop consists of two AND gates and two NOR gates.

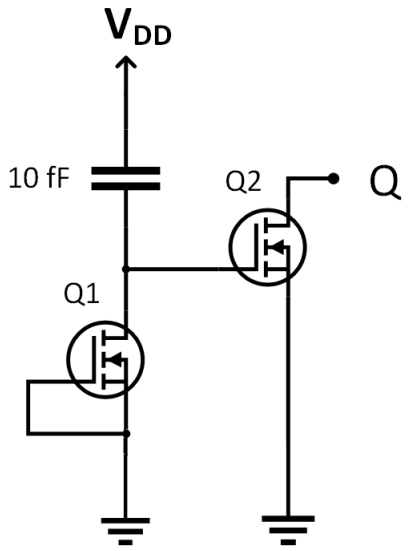

Figure 4.17: Circuit addition to the Toggle Flip Flop's output to ensure it initialises at a low-level state (0 V)

An additional circuit at its output shown in Figure 4.17 ensures that when the circuit is switched on, the initial state of the TFF is low, so that the charge pump would start increasing its output voltage and eventually the duty cycle applied to the AC/DC-to-DC converter would start increasing. If the TFF state initiates

at a high level, then the pump output would remain indefinitely at 0 V which means that the converter never commences its operation. This additional circuit consists of a 10 fF capacitor, connected between the supply voltage and the gate of transistor *Q2*. When the circuit is off, the capacitor discharges through its internal leakage currents and so once the supply voltage is applied, the gate of transistor *Q2* goes to V_{DD} until the capacitor discharges through the leakage currents of the NMOS transistor in the cut-off region *Q1*. Simulations showed that transistor *Q2* is switched on from when the circuit cold starts for a duration of 30 ms thus ensuring that the TFF initiates at a low output state.

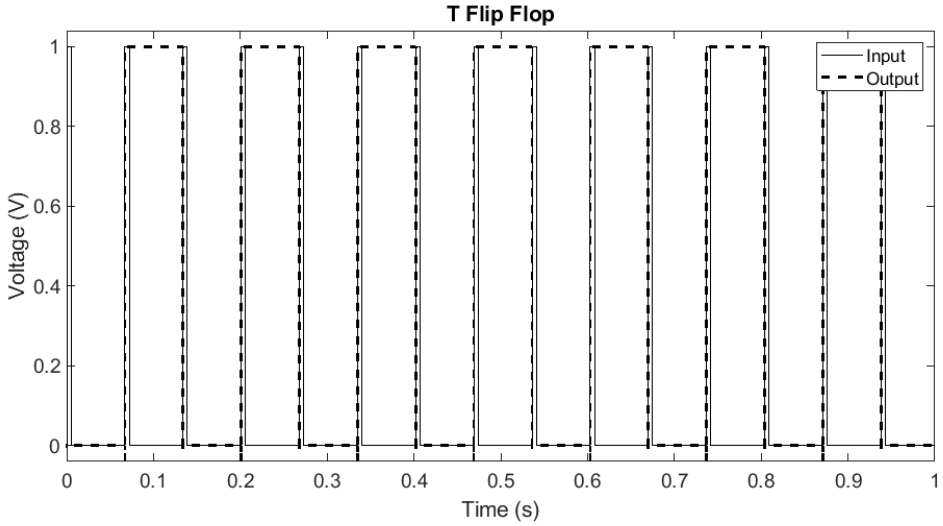

Figure 4.18: Simulation Results of TFF tested with input pulses of 15 Hz

The TFF was simulated individually with 15 Hz pulses at its input and the results are shown in Figure 4.18. The TFF started with a low output state which proves that the circuit implemented to initiate the flip flop at this specific state is working as expected. The TFF consumes an average power of 13.7 pW.

4.1.7 200 kHz Sawtooth Generator

The sawtooth generator is required for the generation of the Pulse Width Modulation (PWM) signal to be applied to the gates of the high voltage NMOS transistors in the switch mode AC/DC-to-DC converter. A sawtooth wave having a voltage ranging from 0 V and 1 V at a frequency of 200 kHz was needed. The switching frequency at which the converter is operated is decided on several factors and following a number of simulations, the switching frequency was decided after a compromise between ripple voltages, switching losses and component sizing (particularly that of the inductor) was made. The design of the sawtooth generator is somewhat like that of the 15 Hz oscillator. The initial part of the circuit consists of a 200 kHz oscillator implemented by means of a Schmitt inverter, an inverter designed to have a low slew rate and an inverter with the discharging part being current starved by a current mirror to control the current at which the 200 fF timing capacitor discharges.

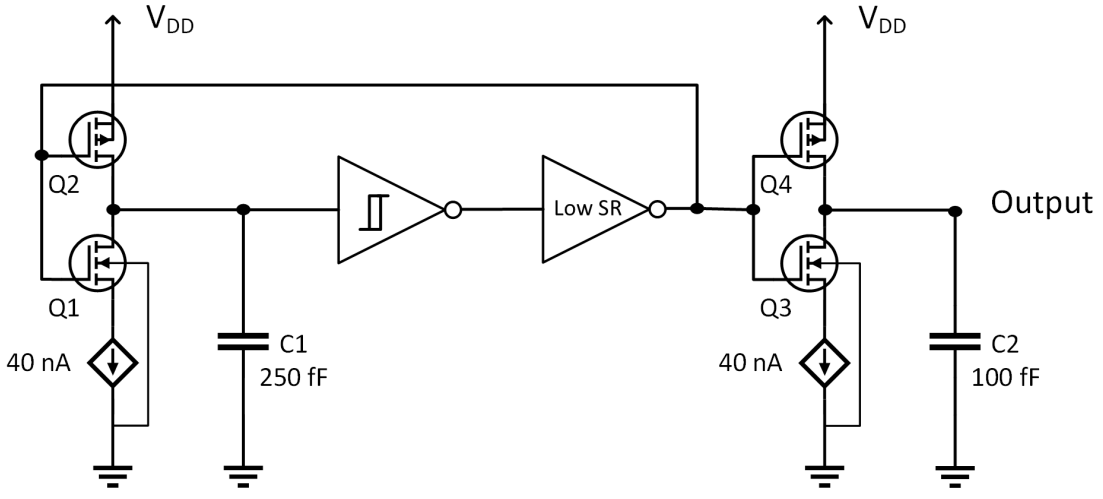

Figure 4.19: Initial Design Schematic Diagram of 200 kHz Sawtooth Generator

The initial design is shown in Figure 4.19 in which the final part of the circuit reconstructs a sawtooth output by using the 200 kHz pulses from the oscillator. When the oscillator's output is 0 V, capacitor C2 is discharged at a constant

current controlled by a current mirror from the same self-biased current reference circuit which generates a constant current of 1.6 nA (refer to Section 4.1.2). A constant current discharges the timing capacitor C1 at a constant voltage rate. When the oscillator's output is 0 V, capacitor C2 charges directly to 1 V via a minimum size PMOS transistor. The current at which capacitor C2 is discharged, was set to exactly drop to 0 V before the clock pulse is over. This current is set with the sawtooth generator output connected to the comparator so that the input capacitance of the inverting terminal is taken in consideration. Although this oscillator reached the required output at typical conditions, when it was analysed at various temperature and corner conditions, the sawtooth output varied substantially, in some cases even losing the sawtooth shape. This happened because of mismatches between the initial part of the circuit, generating the clock pulses and the final part of the circuit, generating the sawtooth wave. For this reason, a more robust design had to be employed.

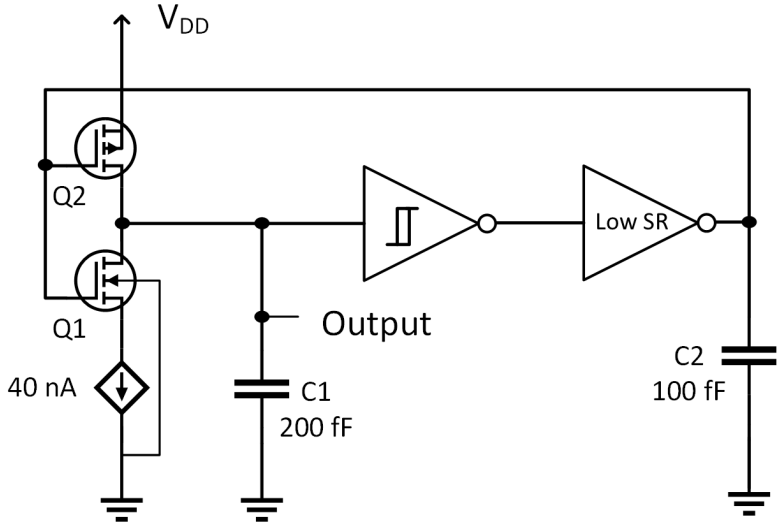

Figure 4.20: Schematic Diagram of final design of 200 kHz Sawtooth Generator

The final design shown in Figure 4.20 was improved by generating the sawtooth wave directly at the timing capacitor *C1* which is now reduced to 200 fF. The implemented Schmitt inverter circuit is shown in Fig. 4.4. It is designed to have

a V_{IL} as close to 0 V as possible and, since the inverter has a low slew rate and a capacitive load of 100 fF, the current starved inverter would continue discharging capacitor *C1* for 50 ns after the Schmitt inverter changes its state. The timing capacitor is charged in 20 ns which is less than 1 % of the full cycle. Hence, the frequency of the oscillator is mainly determined by the discharging current, the timing capacitor, and the hysteresis values of the Schmitt inverter, which are 0 V and 1 V [13].

$$I = C\frac{\delta V}{\delta t}I = 200fF \times \frac{1V}{5\,\mu s} = 40\text{nA} \tag{4.6}$$

A constant current of 1.6 nA is generated by the same self-biased current reference circuit used by the 15 Hz oscillator. Such low current was decided for minimal energy losses. This current had to be mirrored by a scaling factor of 25 to obtain the 40 nA discharging current. It was ensured that the sawtooth waveform reaches the maximum value of the charge pump output voltage (1 V) at all operating temperatures and corner conditions, to prevent the output duty cycle from reaching 100%. Additionally, it was ensured that, across various process and temperature variations, the sawtooth generator does not have a dead-band at 0 V, as this limits the lowest PWM duty cycle which can be obtained. This, thus limits the operation of the boost converters at specific input and output voltages which require a low duty cycle. It is preferable that the sawtooth wave does not reach 0 V rather than having a dead-band at 0 V. The Schmitt inverter, like the one shown in Fig. 4.4, was designed to have $V_{IL} = 90$ mV in typical conditions, by adjusting the aspect ratios of transistors *Q4* and *Q5*. V_{IH} was set to 800 mV in typical conditions. This was achieved by adjusting the aspect ratios of transistors *Q2* and *Q6*. The output of the sawtooth generator simulated at 27 °C with typical conditions is shown in Fig. 4.21 [13].

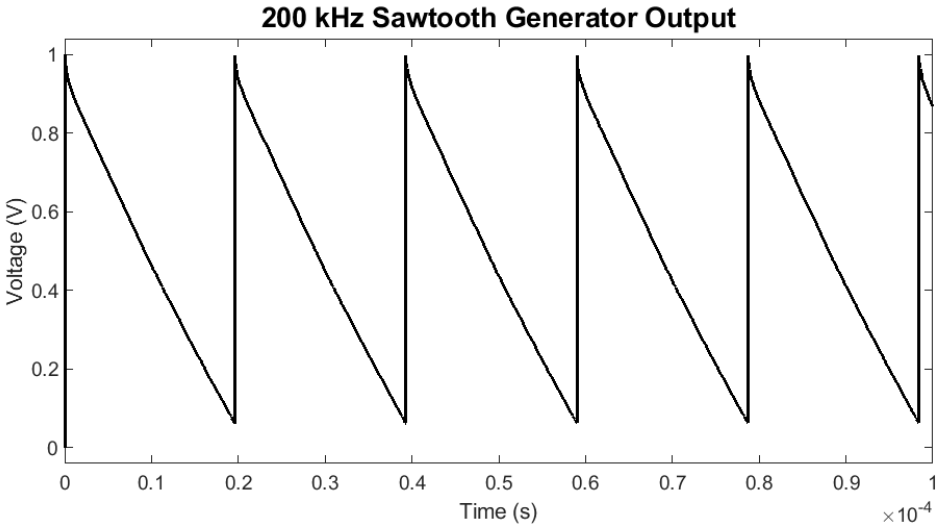

Figure 4.21: Sawtooth Generator Output

The sawtooth wave was required to reach the value of 1 V during all operating conditions because once it is compared to a reference voltage which can reach a voltage close to 1 V, would result in a 100 % duty cycle which may damage the switching devices in the AC-DC Boost converters once the inductor reaches saturation. Another measure for the duty cycle not to reach 100 % was taken in the charge pump circuit which is explained in Section 4.1.8. It is preferable for the sawtooth wave to reach 1 V and having a dead-band at this voltage than not reaching the 1 V. A dead-band at 1 V is beneficial because this results in a limited maximum duty cycle less than 100 % which is essential in all Boost converters controllers.

Additionally, the sawtooth generator throughout all operating conditions, should not have a dead-band at 0 V which would limit the lowest duty cycle which can be achieved in the PWM thus limiting the operation of the AC-DC Boost converters at specific input and output voltages which require a short duty cycle. It would be preferable for the sawtooth wave not to reach 0 V rather than having a dead-band at 0 V.

The linearity of the sawtooth wave and its frequency are of less importance than the two conditions mentioned above because the MPPT would still work efficiently even if the frequency and linearity of the sawtooth generator varies. The switching transistors in the AC-DC converters can work at a switching frequency even in the MHz range. Higher frequency would result in higher switching losses and lower frequency would result in higher ripple currents and voltages, but the converter still operates correctly.

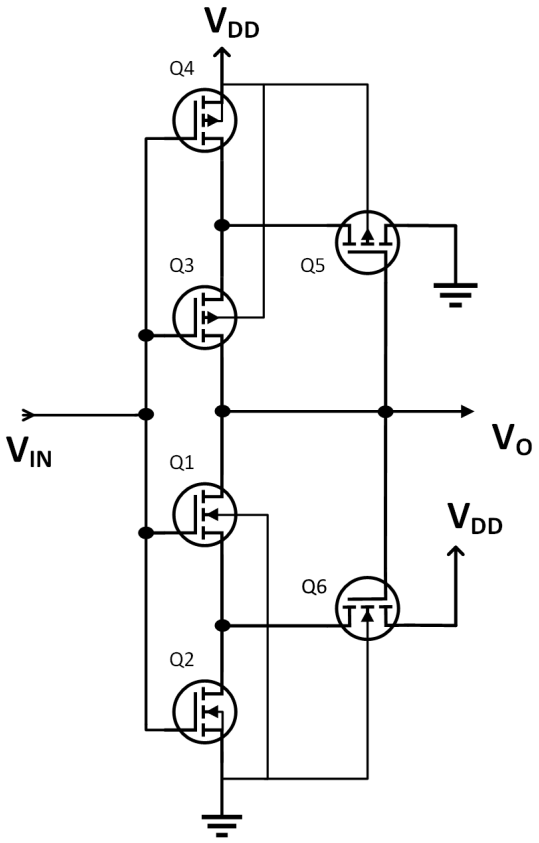

Figure 4.22: Schmitt Inverter Circuit Diagram [91]

The Schmitt inverter's circuit shown in Figure 4.22 is the same as the one used in the 15 Hz clock, but with different transistor sizing. It is designed to have its lower triggering voltage V_{IL} as close to 0 V as possible. Its V_{IL} is 90 mV in typical conditions. The channel width of transistor *Q5* was increased to 3 µm and the

channel length of transistor *Q4* was increased to 1 µm. For the Schmitt inverter to have a good slew rate, the channel width of transistor *Q3* was increased to 0.8 µm. The higher triggering voltage V_{IH} is 800 mV in typical conditions. This was achieved by increasing, both the channel width of transistor *Q6* and the channel length of transistor *Q2* to 5 µm. The output of the sawtooth generator simulated at 27 °C with the typical model library is shown in Figure 4.21.

During its design, the oscillator was tested at various temperature conditions together with corner analysis to obtain a design which is least susceptible to fabrication and environmental changes. This is more challenging due to the low biasing currents involved. The final results are summarised in Table 4.6. The dead-band at 1 V is measured at 0 µs in all corner simulations. Since efficiency is the most important aspect of this whole circuit, one could not opt to improve the temperature correction circuits because such circuits would require higher biasing currents which will eventually consume more power [97]. Hence continuous simulations were carried out to ensure that the operation of the oscillator does not alter substantially. Although the 200 kHz oscillator frequency is the ideal switching frequency of the converter, variations to this frequency do not jeopardise its correct operation, it would just alter its efficiency.

Model Libraries	**Temp (°C)**	**Frequency (kHz)**	**Dead-band @ 0 V (µs)**	**Minimum Voltage (mV)**	**Maximum Voltage (mV)**
Typical	**0**	180	0	16.3	992
	27	190	0	35.7	998
	80	200	0	67.8	997
Worst Speed	**0**	140	2	0	993
	27	150	0.1	0	998
	80	180	0	13	1000
Worst Power	**0**	190	0	62.5	993
	27	200	0	83.1	990
	80	220	0	100	993

Table 4.6: 200 kHz sawtooth generator performance in different temperature and fabrication conditions

From Table 4.6, it can be deduced that the oscillator frequency fluctuates from 140 kHz to 220 kHz in extreme corner analysis conditions. The sawtooth wave reaches 990 mV or higher and no dead-band at this voltage is present in none of the conditions. The sawtooth wave reaches a lower voltage of 100 mV or less and a short dead band of 2 µs or less is only present in the worst speed scenario.

Monte Carlo simulations were also carried out and it showed a standard deviation of 34 kHz. The temperature coefficient and voltage coefficient of the proposed oscillator are 0.17 %/°C and 0.029 %/mV respectively and the circuit occupies an area of 436 μm^2. The sawtooth generator together with the current reference circuit consume 63 nW, which remains constant throughout all temperature range. The variations due to temperature, in the sawtooth wave particularly the minimum voltage, as listed in Table 4.6 do not affect the operation of the switch mode converter and its controller [13]. Table 4.7 compares the specifications of the proposed oscillator with that of existing designs.

Reference	**Technology**	**Min. Supply Voltage (V)**	**Frequency (kHz)**	**Power (nW)**
[89]	65 nm CMOS	1.5	18.5	120
[99]	0.35 µm CMOS	1	80	1140
[100]	65 nm CMOS	1.05	100	41000
[101]	0.35 µm CMOS	1.2	200	84000
This Work	0.35 µm CMOS	1	200	63

Table 4.7: Comparison of the 200 kHz oscillator with the SOA

4.1.8 Charge Pump

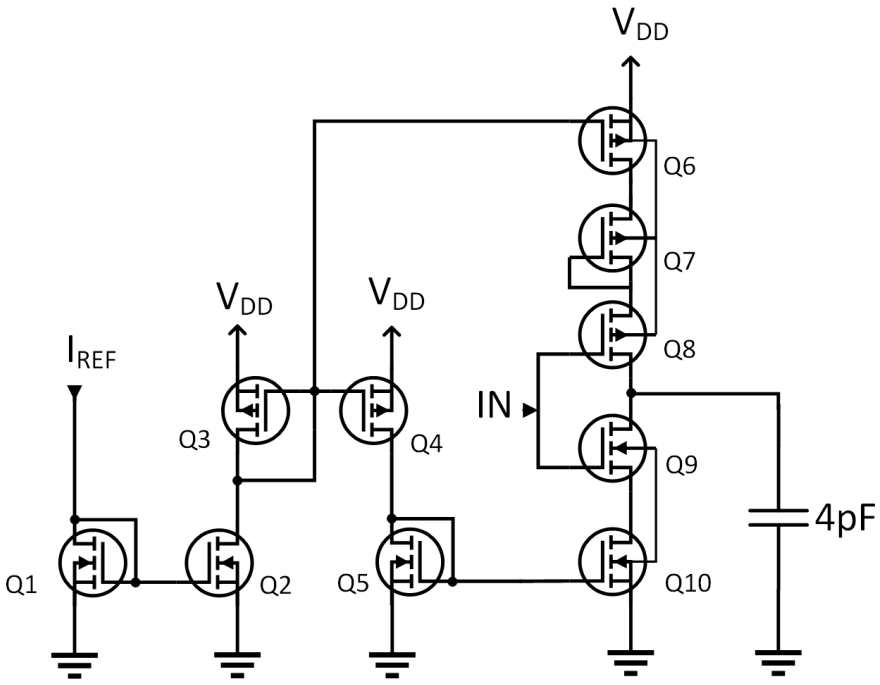

Figure 4.23: Circuit diagram of charge pump block

Transistor Name	**Width**	**Length**
Q1	12 µm	1 µm
Q2	1 µm	1 µm
Q3	12 µm	1 µm
Q4	2 µm	1 µm
Q5	1 µm	1 µm
Q6	2 µm	1 µm
Q7	2 µm	0.5 µm
Q8	0.4 µm	0.35 µm
Q9	0.4 µm	0.35 µm
Q10	4 µm	1 µm

Table 4.8: Transistor sizes of charge pump block

The charge pump shown in Figure 4.23 either increases or decreases its output voltage depending on the state of the TFF. The transistor sizing of this block are listed in Table 4.8. The output voltage determines the duty cycle supplied to the gates of the transistors in the AC-DC converter. The charge pump varies the voltage by either charging or discharging a 4 pF capacitor at a constant current rate. The response time of the converter is very slow mainly because the output currents from the energy harvesters are very low compared to the input inductance and the capacitance of the output storage capacitor. The MPPT clock cycle is of 67 ms and the change in output voltage during this period is of less than 5%.

$$I = C\frac{\delta V}{\delta t} = 4pF \times \frac{1V}{2s} = 2pA \tag{4.7}$$

The charge pump is designed to charge and discharge the capacitor at a current of 2 pA. At this current, the charge pump is capable to fully charge or fully discharge

the capacitor in two seconds as calculated using equation (4.7). The constant current charging and discharging is achieved by means of current mirrors from the same constant current reference source of 1 nA. This very low current is achieved in three matched current mirror stages for both the charging and the discharging currents as shown in Figure 4.23.

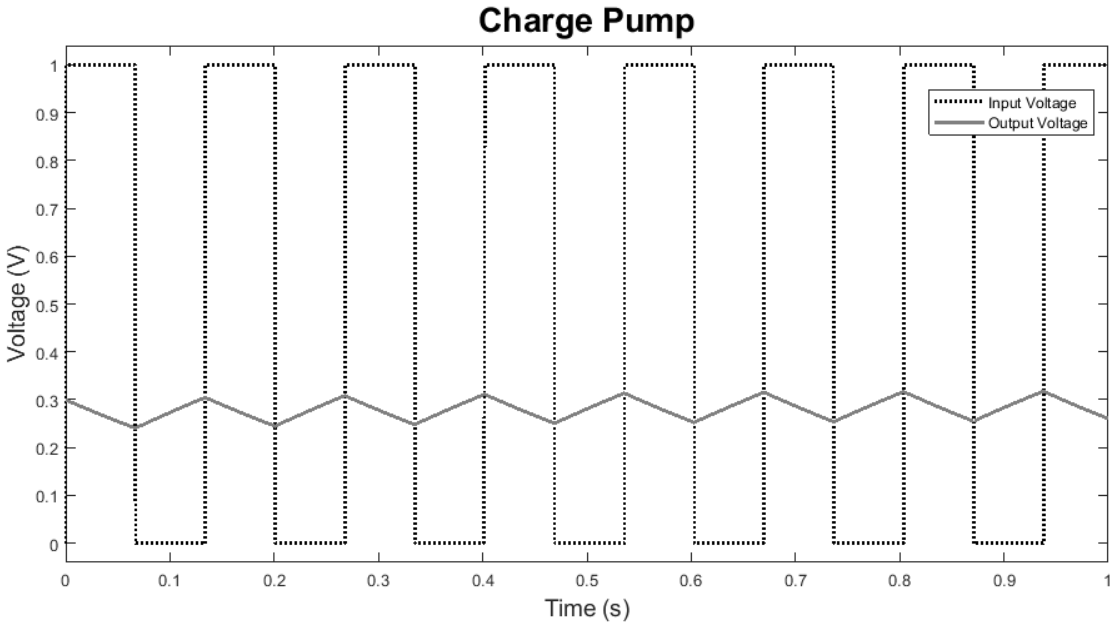

Figure 4.24: Simulation results of the charge pump with an input frequency of 15 Hz

The first two stages mirror down the current by a factor of twelve, and the final stage mirrors scale down the current by a factor of three. The current mirrors were then fine-tuned to counteract the leakage currents due to the very low current involved so that the charging and discharging currents obtained are both 2 pA. In order for the output of the charge pump not to reach a voltage of 1 V which would lead to a duty cycle of 100%, a diode connected PMOS transistor was included in the charging section of the charge pump as shown in Figure 4.23. The charge pump was simulated with an input frequency of 15 Hz as shown in Figure 4.24. The power dissipation of the charge pump is 11.4 pW.

4.1.9 Comparator for PWM Generation

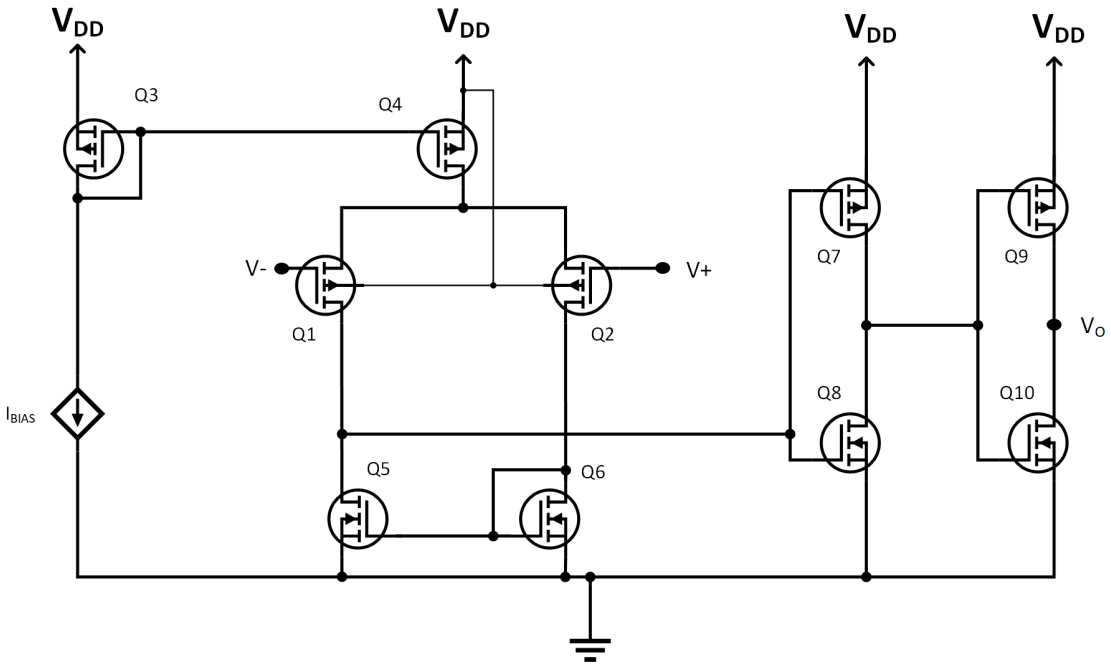

Figure 4.25: PWM generation comparator circuit diagram

The comparator in Figure 4.25 is responsible for the generation of the Pulse Width Modulation to be applied to the gates of the switching devices of the Improved Dual Boost Converter. It compares the charge pump output (non-inverting terminal) with the 200 kHz sawtooth (inverting terminal). It consists of a differential pair which directly drives two successive inverters. The supply voltage of this block is 2 V which is the required gate voltages to achieve a good conversion efficiency in the converter. The PMOS differential pair consumes a power of 10 nW and is capable to work on the full voltage range required from 0 V to 1 V. This differential pair drives two successive inverters with increasing aspect ratios so that the gate capacitance of the switching devices can be charged and discharged at a switching frequency of 200 kHz. The sizes of the transistors in the PWM generation comparator are listed in Table 4.9. Simulation results with a reference voltage of 500 mV and 250 mV are shown in Figure 4.26 and Figure 4.27 respectively. The power dissipation of

this block is 1.08 µW.

Transistor Name	**Width**	**Length**
Q1	2 µm	2.2 µm
Q2	2 µm	2.2 µm
Q5	1 µm	2.4 µm
Q6	1 µm	2.4 µm
Q7	0.4 µm	2 µm
Q8	0.4 µm	1 µm
Q9	8 µm	0.35 µm
Q10	4 µm	0.35 µm

Table 4.9: Transistor sizing of the PWM generation comparator.

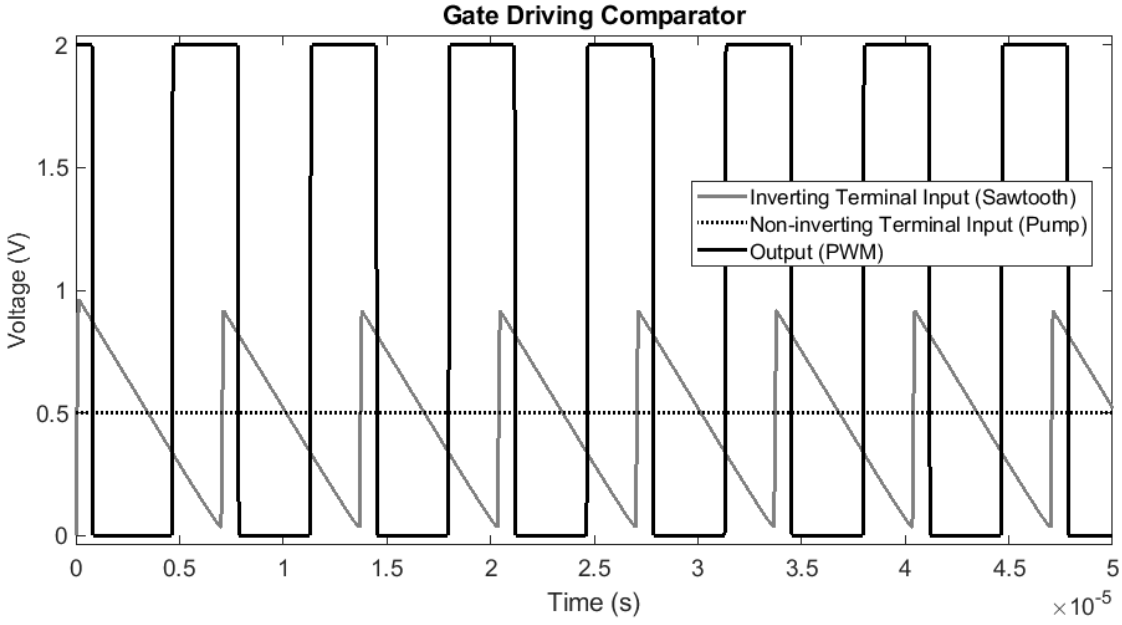

Figure 4.26: Simulation results of PWM generation comparator with a reference input of 500 mV to obtain a 50% duty cycle output

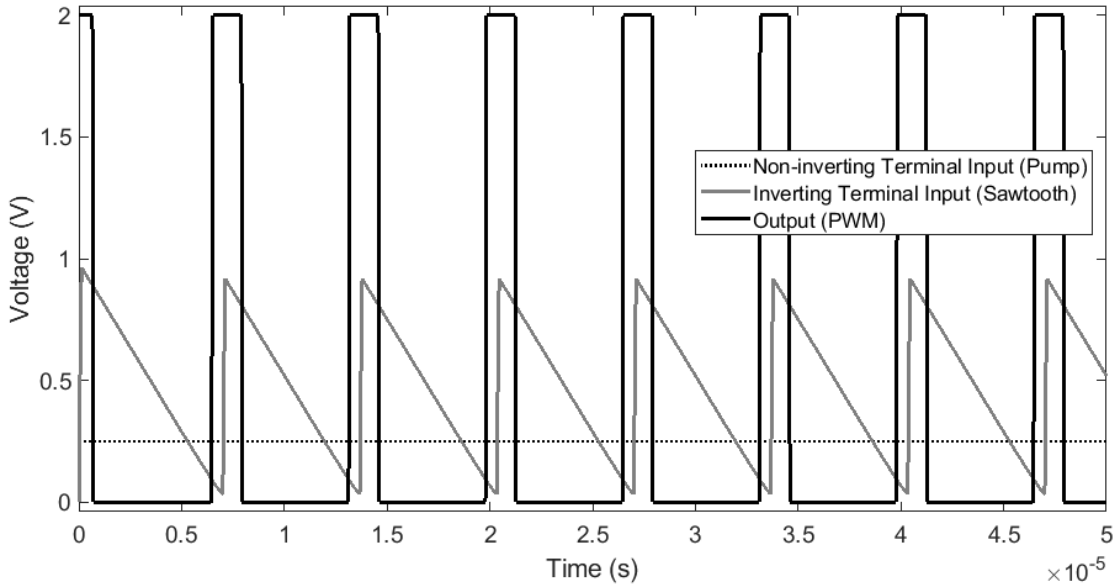

Figure 4.27: Simulation results of PWM generation comparator with a reference input of 250 mV to obtain a 25% duty cycle output

4.1.10 AC/DC-to-DC Dual Boost Converter

Table 3.3 and Table 3.2 show the comparisons between the four direct AC to DC converters considered for this application. The switch mode converter topology chosen to be implemented on-chip for the power conditioning circuit is the improved version dual boost converter which is shown in Figure 4.28. This converter has four modes of operation, two during the positive half cycle and two during the negative half cycle. The modes of operation of this converter are as follows [53];

During the positive half cycle, when the switching transistor Q1 is ON (Mode 1), current flows from the energy harvester, through inductor L (charging inductor L positively), through transistor Q1, forward biases the body diode of transistor Q2 and back to the energy harvester. As soon as the switching transistor Q1 is switched OFF (Mode 2), current from the harvester and inductor forward biases diode D1, charges the output capacitor Co, forward biases the body diode of transistor Q2 and back to the energy harvester.

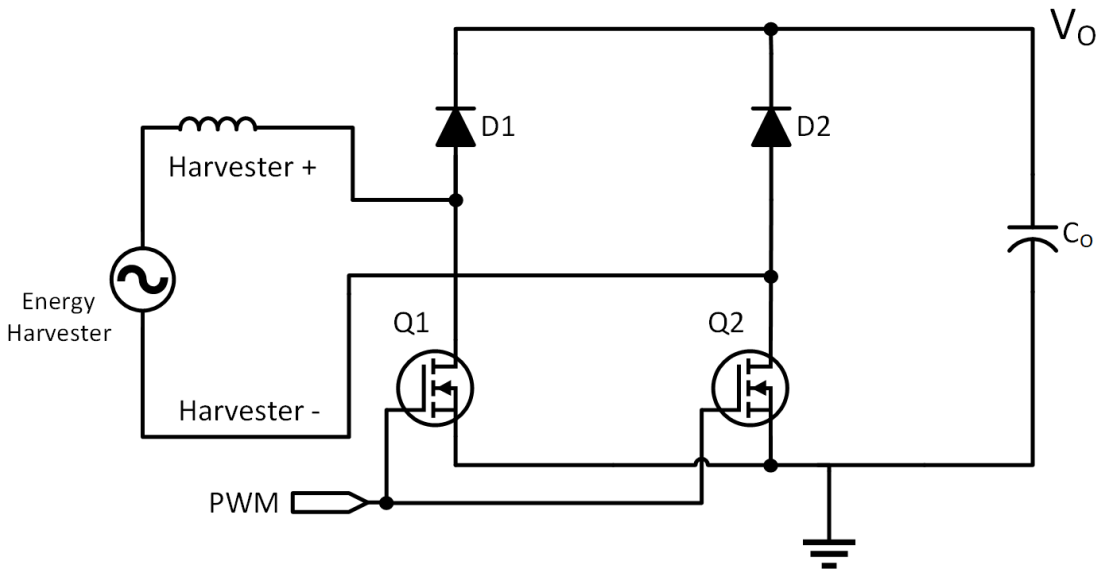

Figure 4.28: Improved Dual Boost converter integrated inside the Power Conditioning circuit [53]

During the negative half cycle, when the switching transistor Q2 is ON (Mode 3), current flows negatively from the energy harvester through transistor Q2, forward biases the body diode of transistor Q1, through inductor L (charging inductor L negatively) and back to the energy harvester. As soon as the switching transistor Q2 is switched OFF (Mode 4), current from the harvester and inductor forward biases diode D2, charges the output capacitor Co, forward biases the body diode of transistor Q1 and back to the harvester and inductor.

The switching transistors Q1 and Q2 both exhibit reverse currents through their respective body diode as part of the converter's normal operation. The forward voltage of the body diode of the high voltage NMOS transistor is 0.7 V and this means that a substantial amount of power is dissipated when allowing current to flow through the body diode only. In [53], a polarity sensing circuit is employed so that during the positive half cycle, only transistor Q1 is operated while during the negative half cycle, only transistor Q2 is operated.

While taking in consideration only the positive half cycle operation of the Dual

Boost converter shown in Figure 4.28,

$$\delta I_{L_{ON}} + \delta I_{L_{OFF}} = 0 \tag{4.8}$$

$$V_L = L\frac{\delta I_L}{\delta t} \tag{4.9}$$

$$\delta I_L = \frac{\delta t}{L} V_L \tag{4.10}$$

Substituting Eq. 4.10 into Eq. 4.8;

$$\frac{DT}{L}\left(V_{IN} - V_L - V_{SW} - V_{PD}\right) + \frac{\left(1-D\right)T}{L}\left(V_{IN} - V_O - V_L - V_D - V_{PD}\right) = 0 \tag{4.11}$$

$$D\left(V_{IN} - V_L - V_{SW} - V_{PD}\right) + \left(1-D\right)\left(V_{IN} - V_O - V_L - V_D - V_{PD}\right) = 0 \tag{4.12}$$

where D is the duty cycle, V_O is the output voltage, V_{IN} is the input voltage, V_{SW} is the voltage across the switching transistor $Q1$, V_{PD} is the voltage drop across the switching transistor's $Q2$ body diode, V_L is the voltage drop on the inductor's series resistance and V_D is the voltage across the diode $D1$.

$$\begin{aligned} DV_{IN} - DV_L - DV_{SW} - DV_{PD} + V_{IN} - V_O - V_L - V_D - V_{PD} \\ -DV_{IN} + DV_O + DV_L + DV_D + DV_{PD} = 0 \end{aligned} \tag{4.13}$$

$$-DV_{SW} + V_{IN} - V_L - V_O - V_D - V_{PD} + DV_O + DV_D = 0 \tag{4.14}$$

$$D\left(V_O - V_{SW} + V_D\right) = V_O - V_{IN} + V_L + V_D + V_{PD} \tag{4.15}$$

$$D = \frac{V_O - V_{IN} + V_D + V_{PD} + V_L}{V_O - V_{SW} + V_D} \tag{4.16}$$

$$\eta = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_{IN} I_{IN}} \tag{4.17}$$

$$I_{IN} = D I_O \tag{4.18}$$

$$\eta = \frac{V_O}{V_{IN} D} \tag{4.19}$$

The duty cycle equation of an ideal Boost converter is

$$D = 1 - \frac{V_{IN}}{V_O} = \frac{V_O - V_{IN}}{V_O} \tag{4.20}$$

The duty cycle in Eq. 4.16 is larger than the ideal duty cycle in Eq. 4.20, so that more current is conducted from the source voltage to compensate for the losses in the inductor's series resistance and the voltage drops in the diodes and transistors. This means that the result of Eq. 4.16 needs to be as small as possible to increase the converter's efficiency.

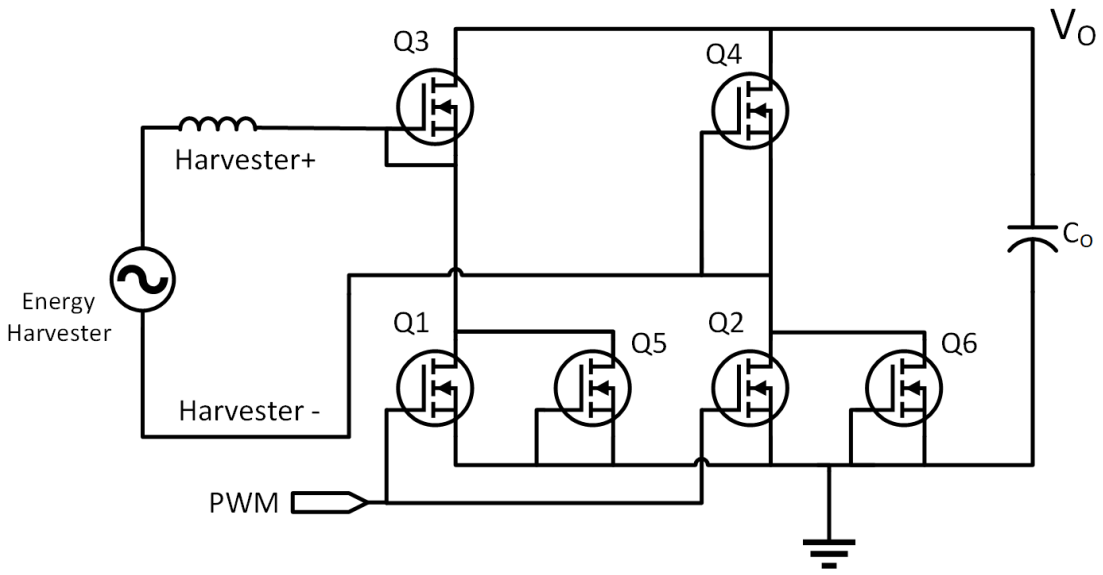

Figure 4.29: Improvements carried out on Dual Boost Converter

The first proposed improvement on the converter was achieved by tying together the gates of transistors Q1 and Q2. This means that both switching transistors switch on simultaneously leading to a much better improvement in efficiency during Modes 1 and 3, mainly because in these modes, the body diodes are never utilised since both transistors are switched on via their gates. Thus in the on cycles, V_{PD} is now replaced by V_{SW}. Moreover, this approach led to a simpler control because there is no need of a polarity sensing circuit and just one PWM generation comparator circuit is enough for both switching transistors. Modes 2 and 4 are the remaining modes of operation where the body diode is still used. The forward voltage of the high voltage NMOS transistor's body diode V_{PD} is 0.7 V whereas the forward voltage of the same transistor diode connected V_D is 0.45 V [94]. Hence to obtain a lower voltage drop, a diode connected transistor is connected in parallel to both transistors Q1 and Q2. This means that in the off cycles, V_{PD} is now replaced by V_D. In CMOS, the simplest most effective way of implementing a diode is by using diode-connected transistors and hence both D1 and D2 are implemented using this technique. The resultant improved converter as implemented and simulated in

Cadence is shown in Figure 4.29. The new four modes of operation are as follows;

During the positive half cycle, when the switching transistors are 'ON' (Mode 1), current flows from the energy harvester, through the externally connected inductor (charging inductor L positively), through transistor Q3, transistor Q2 and back to the energy harvester. As soon as the switching transistors are switched 'OFF' (Mode 2), current from the harvester and inductor forward biases diode-connected transistor Q5, charges the externally connected output storage capacitor, forward biases diode-connected transistor Q7 and back to the energy harvester.

During the negative half cycle, when the switching transistors are 'ON' (Mode 3), current flows in the opposite direction from the energy harvester through transistor Q1, transistor Q2, through the externally connected inductor L (charging inductor L negatively) and back to the energy harvester. As soon as the switching transistors are switched 'OFF' (Mode 4), current from the harvester and inductor forward biases diode-connected transistor Q3, charges the externally connected output storage capacitor, forward biases diode-connected transistor Q6 and back to the harvester and inductor.

Eq. 4.11 changes as follows due to the improvements carried out.

$$\frac{DT}{L}\left(V_{IN} - V_L - 2V_{SW}\right) + \frac{(1-D)\,T}{L}\left(V_{IN} - V_O - V_L - 2V_D\right) = 0 \tag{4.21}$$

$$D\left(V_{IN} - V_L - 2V_{SW}\right) + (1-D)\left(V_{IN} - V_O - V_L - 2V_D\right) = 0 \tag{4.22}$$

where with reference to Figure 4.29, D is the duty cycle, V_O is the output voltage, V_{IN} is the input voltage, V_{SW} is the voltage across the switching transistors $Q1$ and $Q2$, V_L is the inductor voltage drop and V_D is the voltage across the diode connected transistors $Q3$ and $Q4$.

$$\begin{aligned} DV_{IN} - DV_L - 2DV_{SW} + V_{IN} - V_O - V_L - 2V_D \\ -DV_{IN} + DV_O + DV_L + 2DV_D = 0 \end{aligned} \tag{4.23}$$

$$-2DV_{SW} + V_{IN} - V_L - V_O - 2V_D + DV_O + 2DV_D = 0 \tag{4.24}$$

$$D\left(V_O - 2V_{SW} + 2V_D\right) = V_O - V_{IN} + V_L + 2V_D \tag{4.25}$$

$$D = \frac{V_O - V_{IN} + 2V_D + V_L}{V_O - 2V_{SW} + 2V_D} \tag{4.26}$$

The most efficient high voltage transistor in the AMS technology which can operate in the active region with a gate voltage of 2 V at the required conduction current is the one having the thinnest gate oxide layer NMOS50IT. This transistor has a threshold voltage of 0.45 V. The sizes of switching transistors Q1 and Q2 and diode connected transistors Q5 and Q6 are 100 µm wide and 0.5 µm long respectively. These transistors are capable of carrying a current of 26 mA until reaching saturation when operated at a gate voltage of 2 V [94]. Diode connected transistors Q3 and Q4 have an increased width of 150 µm and the same length of 0.5 µm because simulations showed that they exhibit a longer turn-on delay and a higher forward voltage until they start conducting thus affecting negatively the efficiency of the converter.

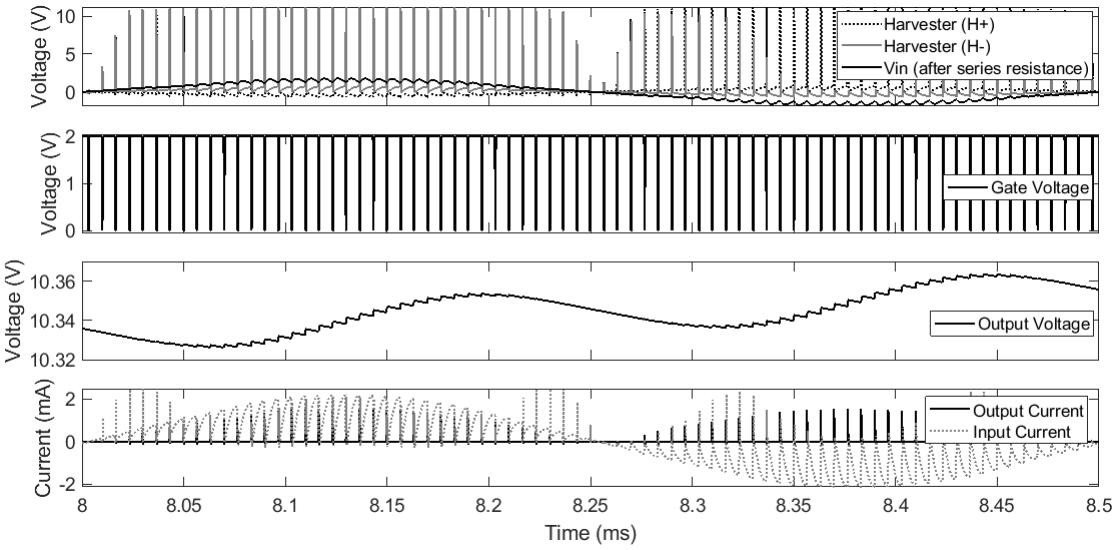

Figure 4.30: Simulation results of one input cycle of the improved dual boost operated at a duty cycle of 95%, switching frequency of 200 kHz, a constant output current of 20 µA, and a 5 V p-p 2 kHz input voltage through a series resistance of 2.5 kΩ.

Figure 4.30 show the operation of the Improved Dual Boost converter when operated with a 5 V peak-to-peak 2 kHz AC input voltage. The ideal operation for such a converter is to vary the duty cycle throughout the input sine wave, so that the average inductor current is sinusoidal and proportional to the input voltage. However, this would require advanced control which cannot be obtained with such low control power dissipation [102].

4.2 Simulation Results

The design of the AC/DC-to-DC converter with MPPT function was carried out one block at a time as detailed above. The block being designed was simulated and tweaked until correct operation was achieved. The circuit blocks were also simulated together with the subsequent connected block so that it is ensured that the current loading of the subsequent circuit did not affect the operation in any

way. Once all circuit blocks were designed and performed satisfactorily, all blocks were simulated together, and the results are shown and discussed further on in this chapter.

Simulations were initially carried out on a circuit level because it is less time consuming and more practical. Consequently, this is a faster approach to tweak and modify the circuits individually until the circuits work as expected. Once all circuit blocks worked as expected, the whole system design was simulated at various input and load conditions. The simulations are very slow and a one second transient circuit simulation takes several days to complete and used up a substantial amount of the computer's storage. This happens because the first part of the circuit operates at a clock frequency of 15 Hz while the final part works at a clock frequency of 200 kHz. This meant that the simulation had to be very long to get enough data for the 15 Hz part of the circuit. However, the simulation was slowed by the part of the circuit clocked at 200 kHz. Simulations showed that all the block circuits operate as expected once connected together. In some simulations, one second was not enough for the output voltage and the MPPT's operation to reach steady state. Furthermore, corner simulations under different temperature conditions were also carried out and the circuit kept working as expected. Several simulations carried out at different input, load and temperature conditions are plotted in the figures below. The conditions at which the circuit was simulated is described in the figure's respective caption. Simulations show that the total power consumption of the complete circuit will be less than 1 µW under normal MPPT and voltage conversion operation.

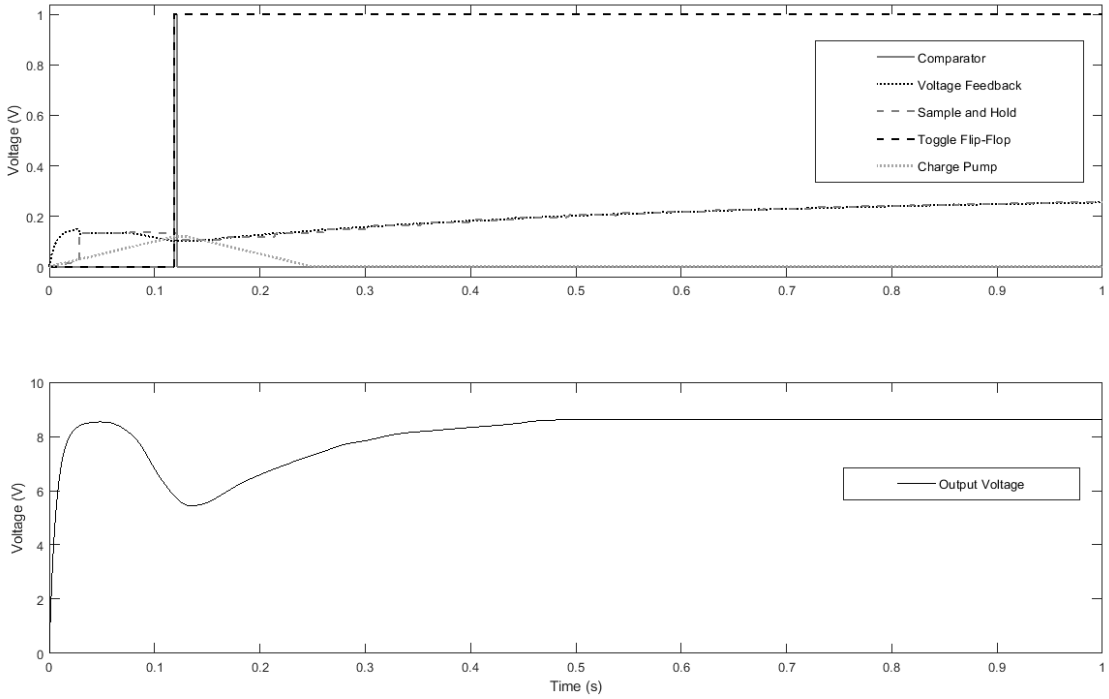

Figure 4.31: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 10 V, a series resistance of 50 kΩ and a constant output current loading of 10 µA

Figure 4.31 shows the circuit operation when simulating an input voltage of 10 V, a series resistance of 50 kΩ and a load current of 10 µA. As expected, the circuit starts up with the TFF's output state at 0 V so that the charge pump's output starts increasing from 0 V. As the converter's duty cycle increases, so does the output voltage. As the output voltage reaches its peak voltage of 8.5 V and starts decreasing again, the clocked comparator generated an output clock pulse to the TFF within 0.05 s which changed its output state to 1 V so that the charge pump's output decreased again.

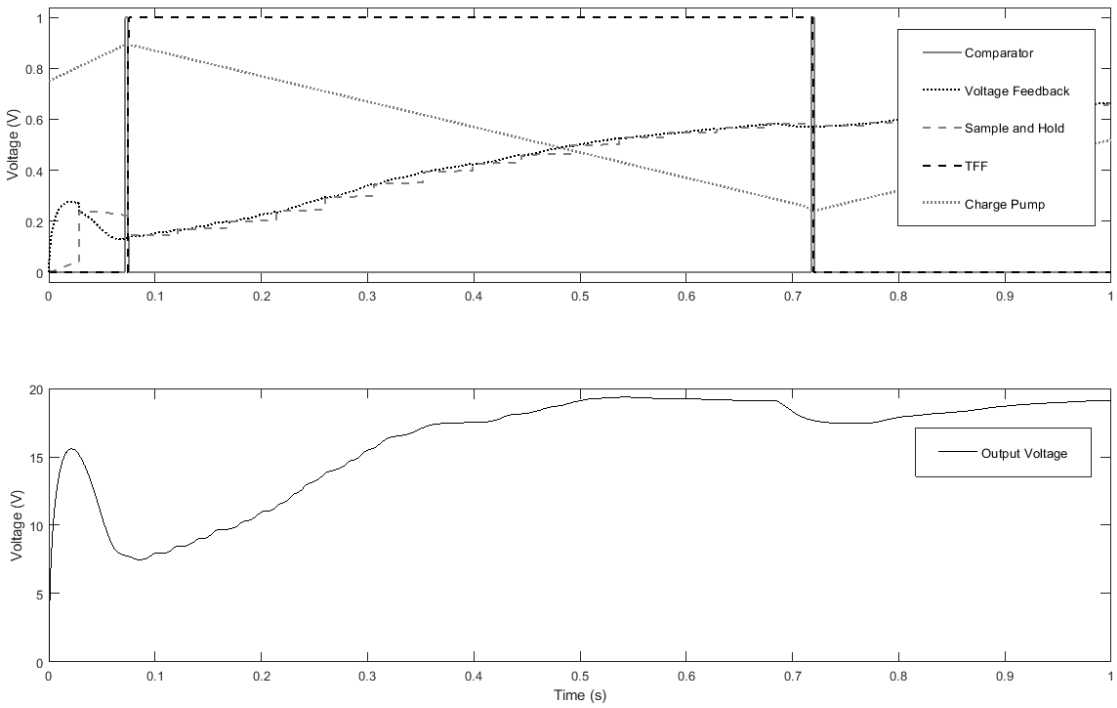

Figure 4.32: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 10 V, a series resistance of 5 kΩ and a constant output current loading of 100 µA

Another simulation was carried out, now with a series resistance of 5 kΩ and a constant output load current of 100 µA. The input voltage and impedance values are of typical energy harvesters. The results are shown in Figure 4.32. When the output voltage decreased, at 0.07 s and 0.72 s, the TFF output state changed as expected. An input voltage of 10 V was boosted to a maximum voltage of 19 V. The end-to-end efficiency of the circuit can be calculated by calculating the maximum power which can be generated from the source and the output power. The maximum power which can be generated is when the load resistance matches the input series resistance of 5 kΩ. At this point the input voltage of 10 V is split evenly across the series resistance and the converter. This means that the maximum input power which can be achieved is given by Equation (4.27) whereas the output power can be calculated simply by Equation (4.28). Hence the maximum achievable

power is 5 mW whereas the output power is 1.9 mW.

$$P_{IN} = \frac{V_{IN}^2}{4R_{IN}} \tag{4.27}$$

$$P_O = V_O I_O \tag{4.28}$$

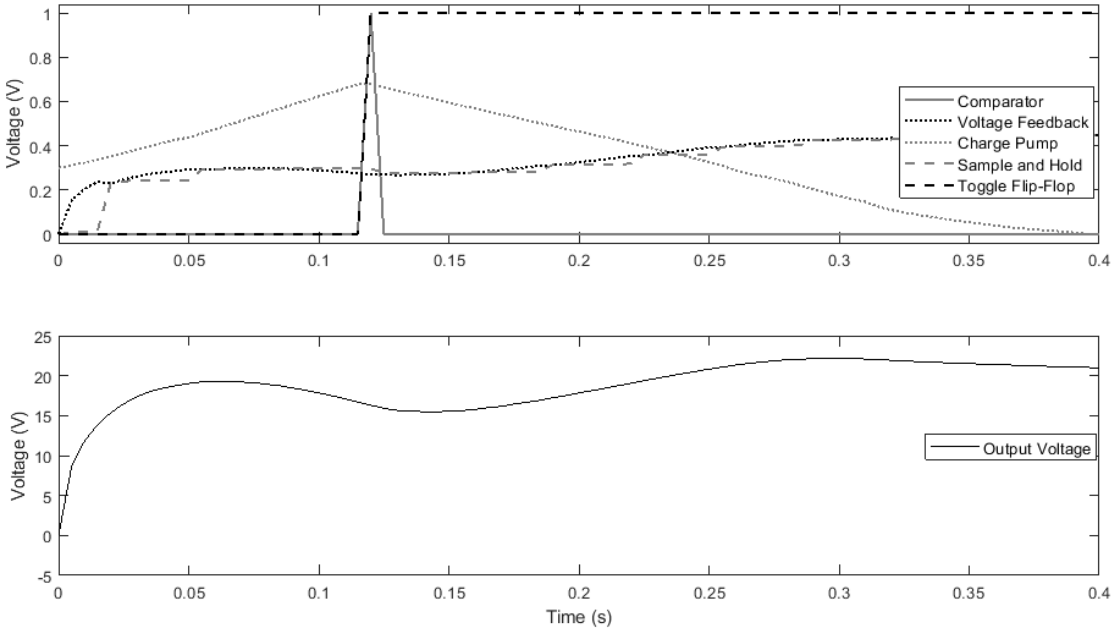

Figure 4.33: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 10 V, a series resistance of 10 kΩ and a constant output current loading of 50 µA

Figure 4.33 plots the results obtained when simulating the circuit at an input voltage of 10 V, an input resistance of 10 kΩ and an output load current of 50 µA. The maximum achievable input power in this simulation is 2.5 mW and the peak output power generated was 1.1 mW.

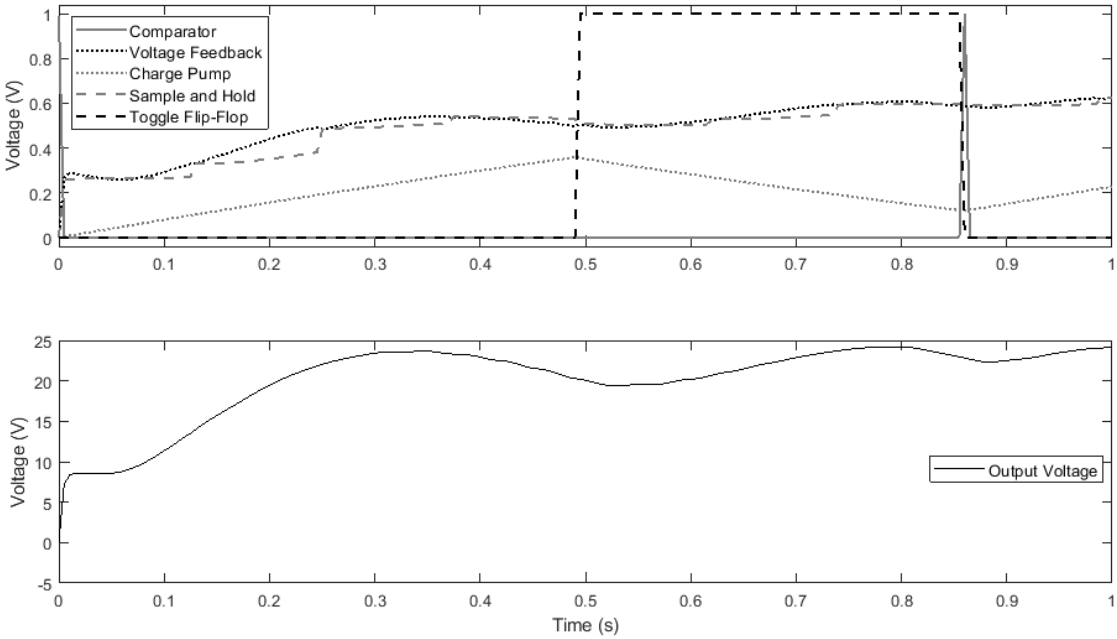

Figure 4.34: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 10 V, a series resistance of 25 kΩ and a constant output current loading of 25 µA

Simulation results of the circuit operated with an input voltage of 10 V, series resistance of 10 kΩ and output current of 50 µA are shown in Figure 4.34. Maximum achievable power and peak output power are calculated to be 2.5 mW and 1.3 mW respectively. The output voltage is settling at 25 V.

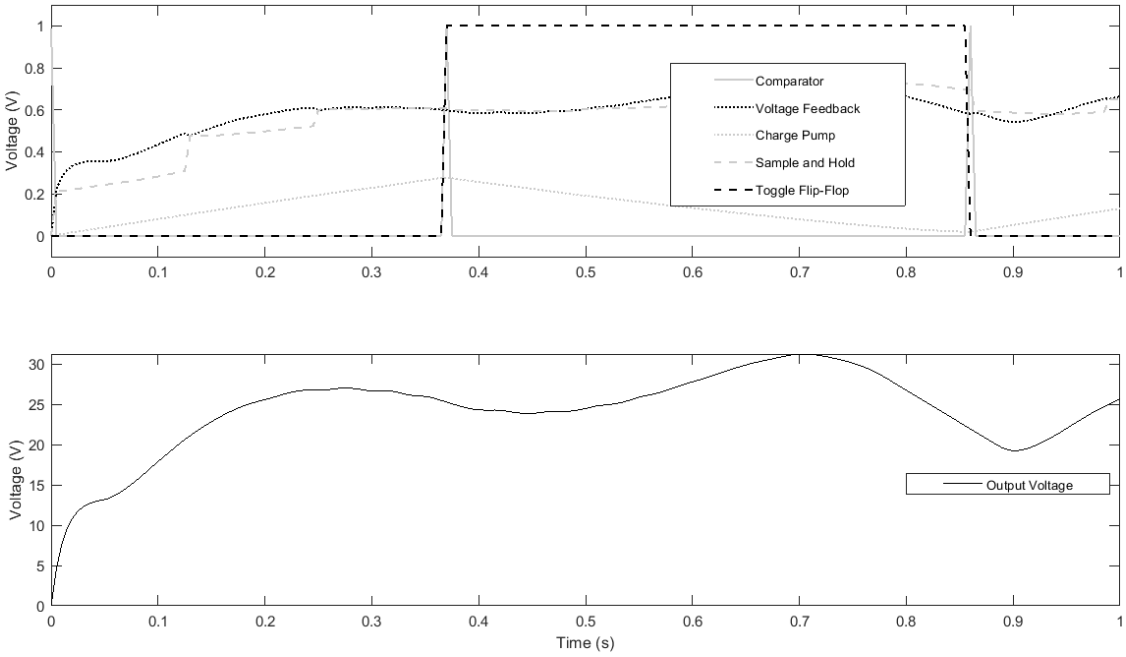

Figure 4.35: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 15 V, a series resistance of 112.5 kΩ and a constant output current loading of 8 µA

Figure 4.35 plots the output results when simulating with a higher input voltage of 15 V, series resistance of 112.5 kΩ and output current of 8 µA. Maximum achievable input power in this simulation is 500 µW and the peak output power peaked at 260 µW. At 0.8 s, the converter suffered from a runaway condition and the voltage dropped from 30 V to 20 V. This usually happens when the input power cannot sustain the load power. As a result as the input voltage drops, the converter tries to drain more current to try to sustain the same output power. This leads to an even higher voltage drop thus leading to a runaway condition. The converter managed to recover from this voltage drop at 0.9 s.

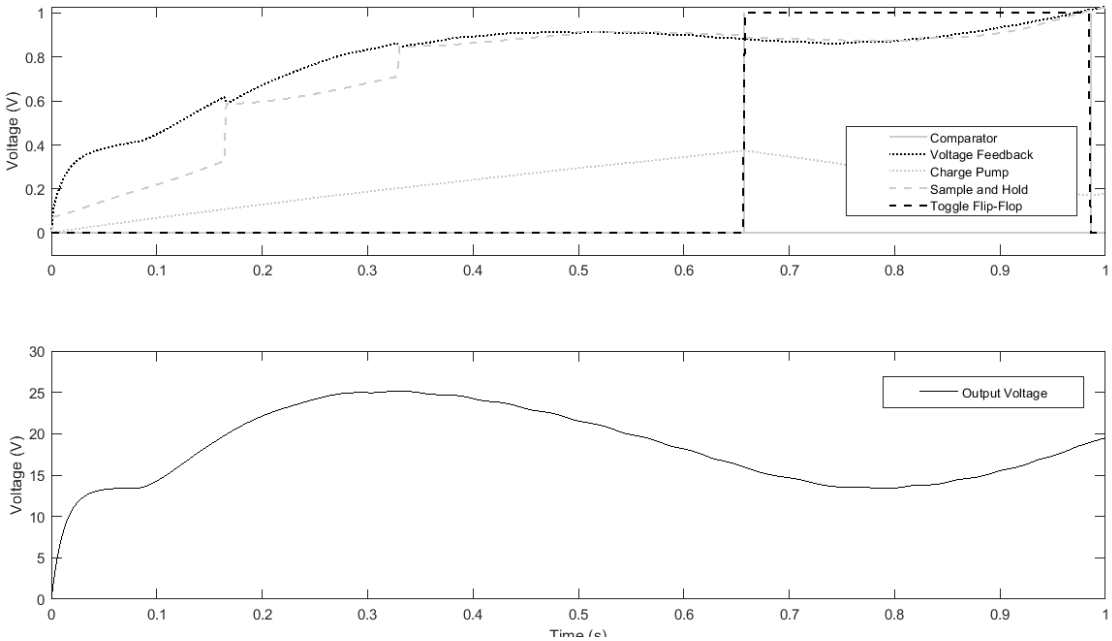

Figure 4.36: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a temperature of 80 °C, an input DC voltage of 15 V, a series resistance of 112.5 kΩ for a maximum achievable input power of 500 µW and a constant output current loading of 8 µA

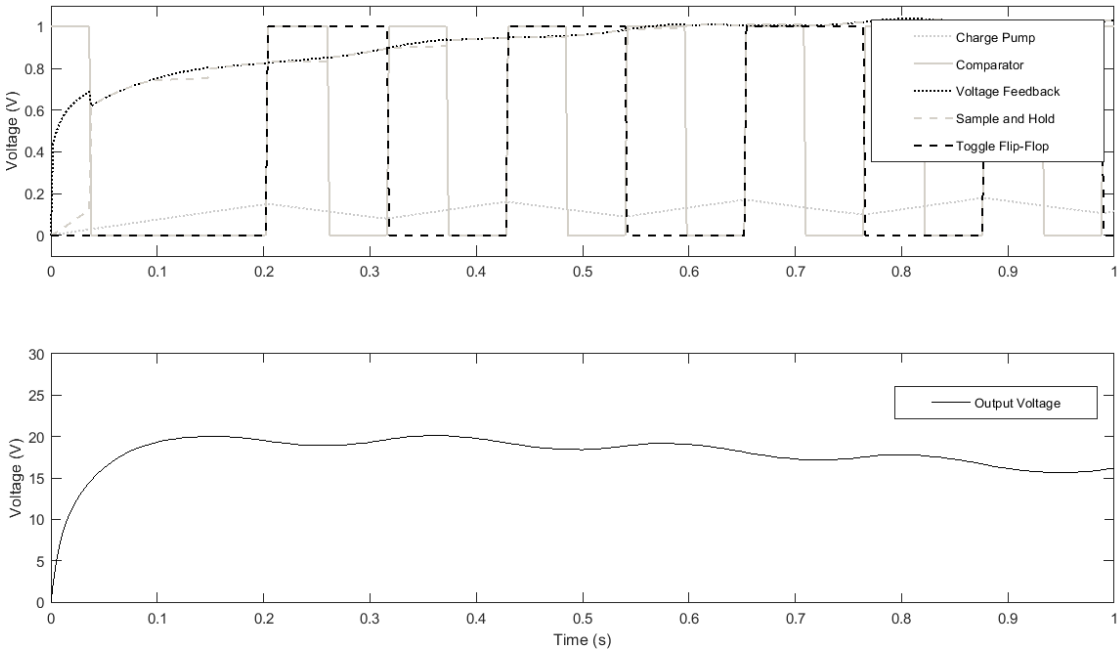

Figure 4.37: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at a temperature of −20 °C, an input DC voltage of 15 V, a series resistance of 112.5 kΩ and a constant output current loading of 5 µA

Once the simulations with typical temperature conditions of 27 °C resulted in satisfactory response, simulations varying these optimal temperature conditions were also carried out. Figure 4.36 shows the output results from a simulation carried out at temperature of 80 °C, whereas Figure 4.37 carries out the same simulation but at a temperature of −20 °C. One can note that the ideal MPPT clock frequency of 15 Hz was slightly affected but this did not jeopardize the correct MPPT operation.

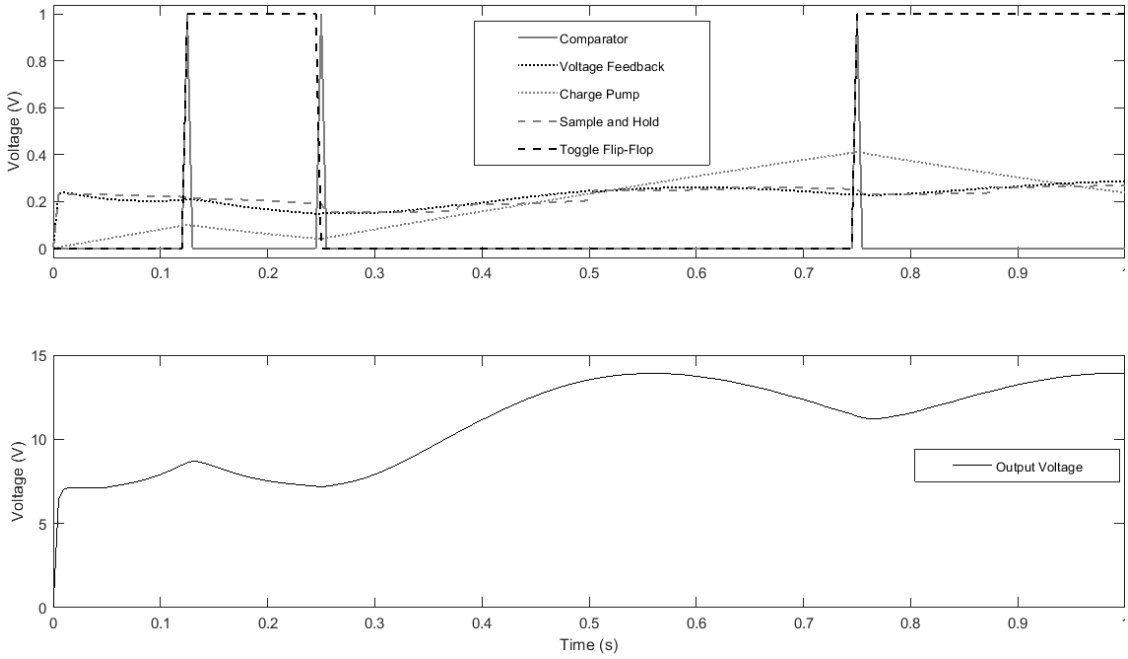

Figure 4.38: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at an AC peak input voltage of 10 V, a series resistance of 1 kΩ and a constant output current loading of 50 µA

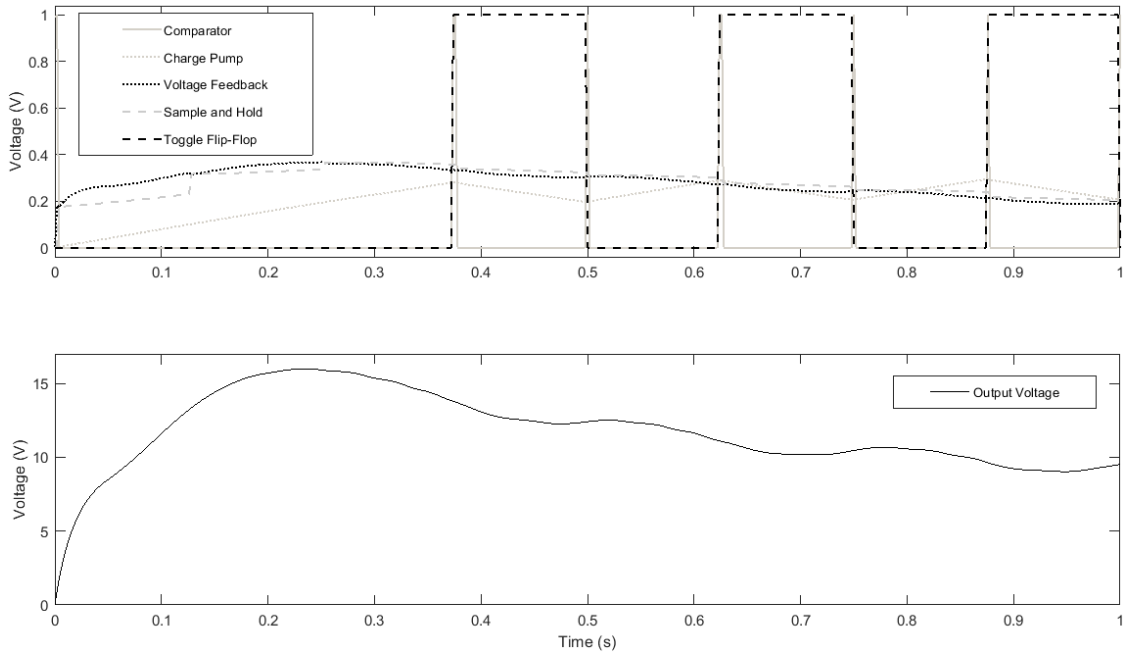

Figure 4.39: Simulation Results of complete AC/DC-to-DC Converter with MPPT function operated at an AC peak input voltage of 21.2 V, a series resistance of 225 kΩ and a constant output current loading of 5 µA

The circuit was also simulated with an AC input having an rms voltage of 7.07 V at a frequency of 1 kHz. The respective simulation results are plotted in Figure 4.38. A higher input AC voltage of 15 V rms was simulated and the results are plotted in Figure 4.39. These two simulations confirm that both the MPPT and the improved dual boost AC/DC-to-DC converter are compatible with AC input voltages.

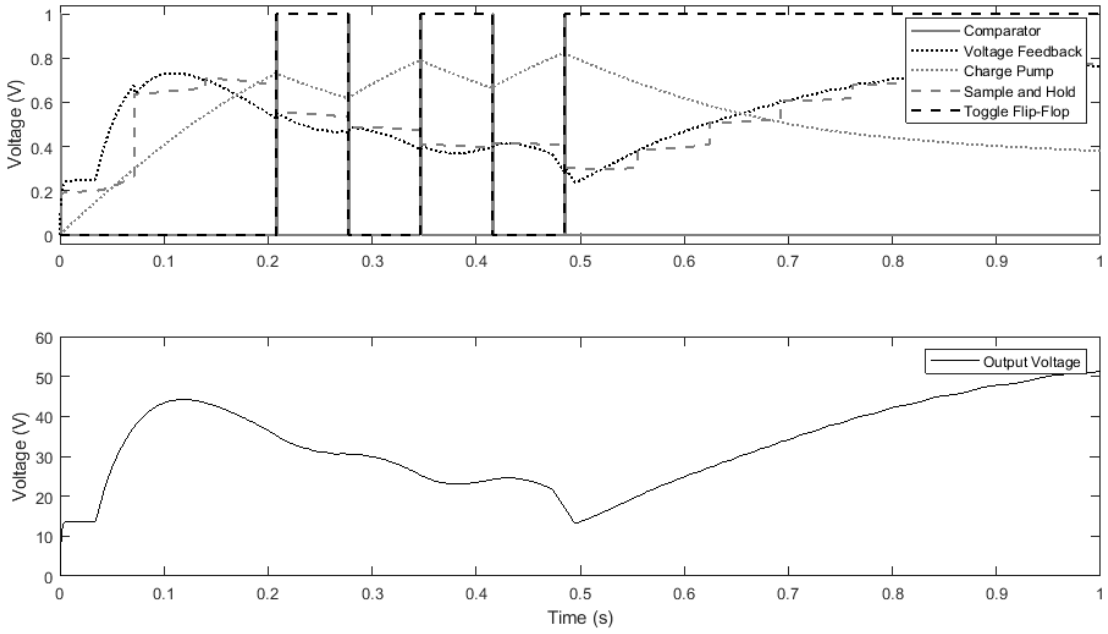

Figure 4.40: Worst power corner simulation results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 15 V, a series resistance of 112.5 kΩ and a constant output current loading of 5 µA

The final simulations to confirm an integrated circuit's robustness was to carry out corner analysis simulations which are carried out at the extremes of power and speed fabrication conditions which fall within the fabrication tolerances. Figure 4.40 and Figure 4.41 report the simulations of the circuit at worst power fabrication conditions and worst speed fabrication conditions respectively. These simulations also yielded correct operations. Further simulations combining both temperature and fabrication changes concurrently were also carried out so that any changes

in the operation or weaknesses in the circuit design were exposed. However, the changes that were noted did not affect the circuit's operation. Due to the circuit complexity, Monte Carlo simulations could not be carried out on the complete MPPT circuit. Therefore, these were done only on the 15 Hz clock and the 200 kHz sawtooth generator.

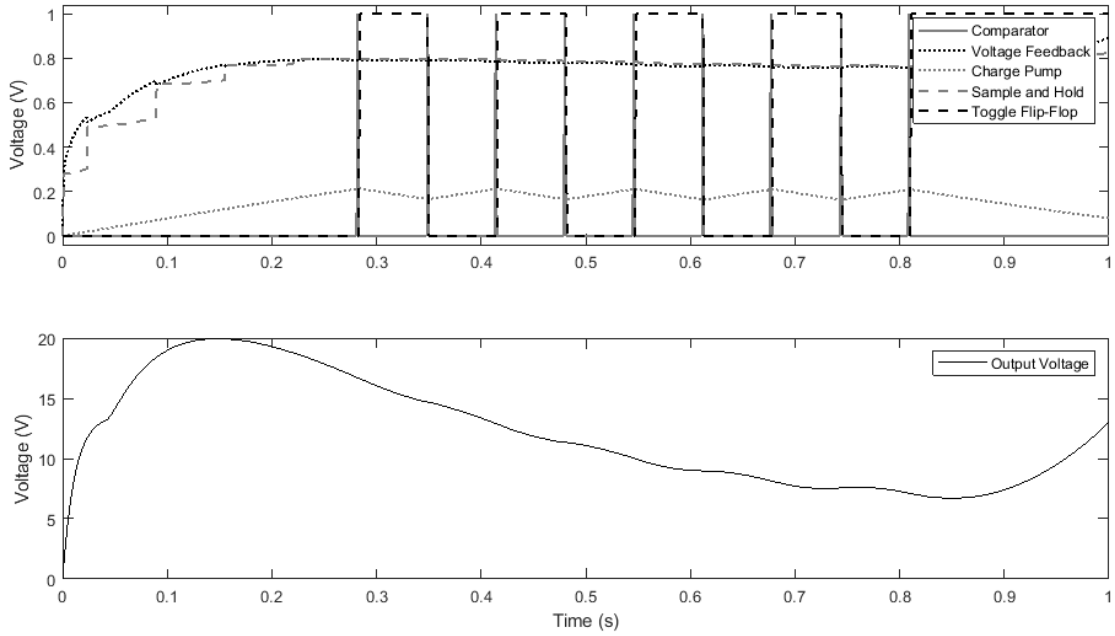

Figure 4.41: Worst speed simulation results of complete AC/DC-to-DC Converter with MPPT function operated at a DC input voltage of 15 V, a series resistance of 112.5 kΩ and a constant output current loading of 5 µA

The simulations carried out on the whole system show that AC/DC-to-DC converter and the MPPT controller work as expected. The MPPT is changes the duty cycle of the converter so that maximum output voltage across the storage capacitor is obtained. Simulations took a substantial amount of time just to carry out a one-second-long full circuit simulation. In some cases, one second was not enough to reach stability. However, it still can be deduced that the MPPT is adjusting towards maximum power point.

4.3 Experimental results of AC/DC-to-DC converter with MPPT function

Following the circuit design and simulation at various temperature, voltage and process conditions [6, 13], circuit layout, and post layout simulations, the circuit was fabricated. The circuit layout is described in Appendix B. The layout includes four high voltage pads and sixteen low voltage pads as shown in Figure 4.42. Most of these pads were included to increase the testability of the prototype circuit. Pads were included at the input and output of every block, so that each individual block could be monitored externally. The dimension of the integrated circuit, including the pads, is 1271 µm by 1347 µm, that is an area of 1.7 mm^2. The active circuit covers an area of 0.11 mm^2. The integrated circuit was packaged in the DIL24 package as shown in Figure 4.43. A testing board was designed and developed to supply the required bias currents and operate the circuit to be able to supply voltages and read signals to monitor its operation.

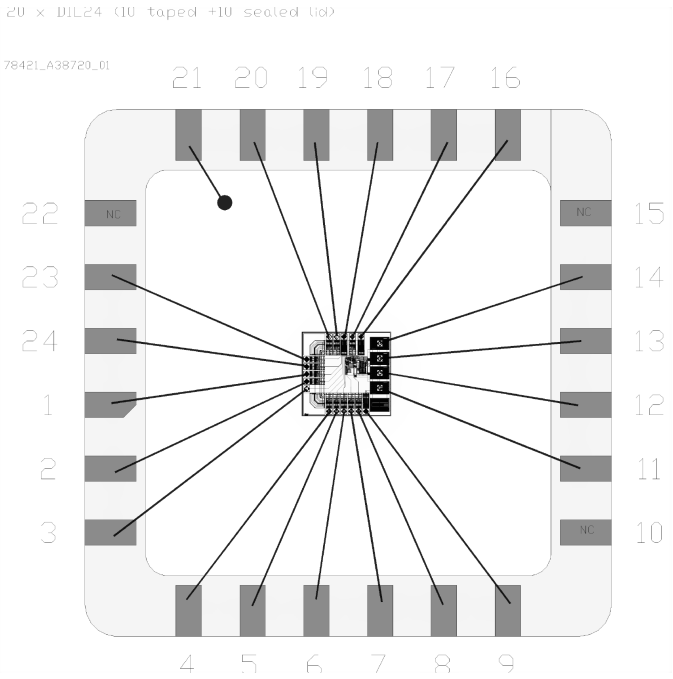

Figure 4.42: Bonding diagram of the integrated circuit to a DIL24 package

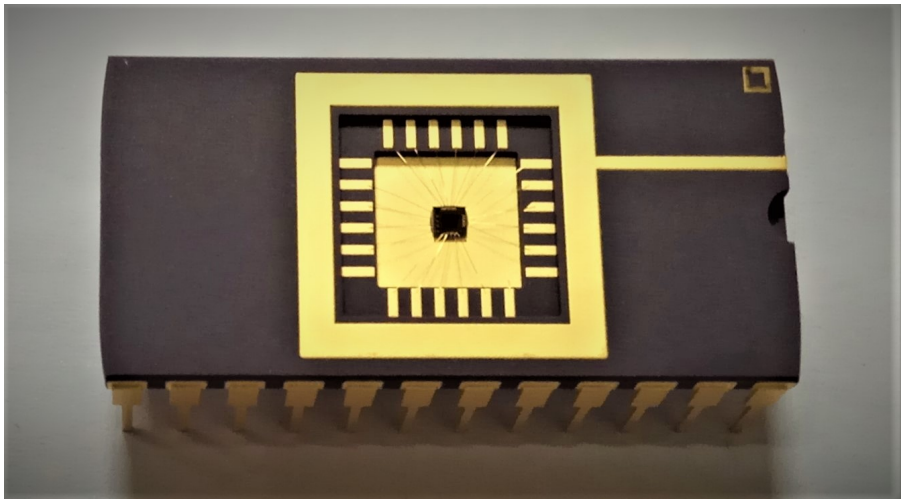

Figure 4.43: Picture of fabricated integrated circuit packaged in taped lid DIL24 package

Post-layout simulations were carried out to assess the effect of the pads on the total power consumption and the functionality of the circuit blocks. This was particularly relevant for those pads switching at a high frequency such as the sawtooth generator and gate driver pads since pad loading tend to slow their response time. Post layout simulations of the circuit only including the essential pads, showed a static power consumption of 1.2 µW. However, the same post layout simulation shows an increase in power dissipation to 8.1 µW when all the redundant testing pads are included. This happens because slight modifications to the circuitry had to be carried out, particularly the current biasing for the oscillators to maintain the designated oscillating frequency. The actual measured power consumption of the fabricated integrated circuit was found to be 10 µW which is slightly higher than the consumption obtained in post layout simulations mainly because the sawtooth generator oscillated slightly higher than 200 kHz. However, if this circuit was fabricated without the redundant testing pads, the power consumption is expected to drop back to below 2 µW. Although the pads did not contribute to any significant losses due to leakage currents, their capacitance increased substantially the power consumption of the sawtooth generator and gate

driving comparator because their output pads oscillate at 200 kHz.

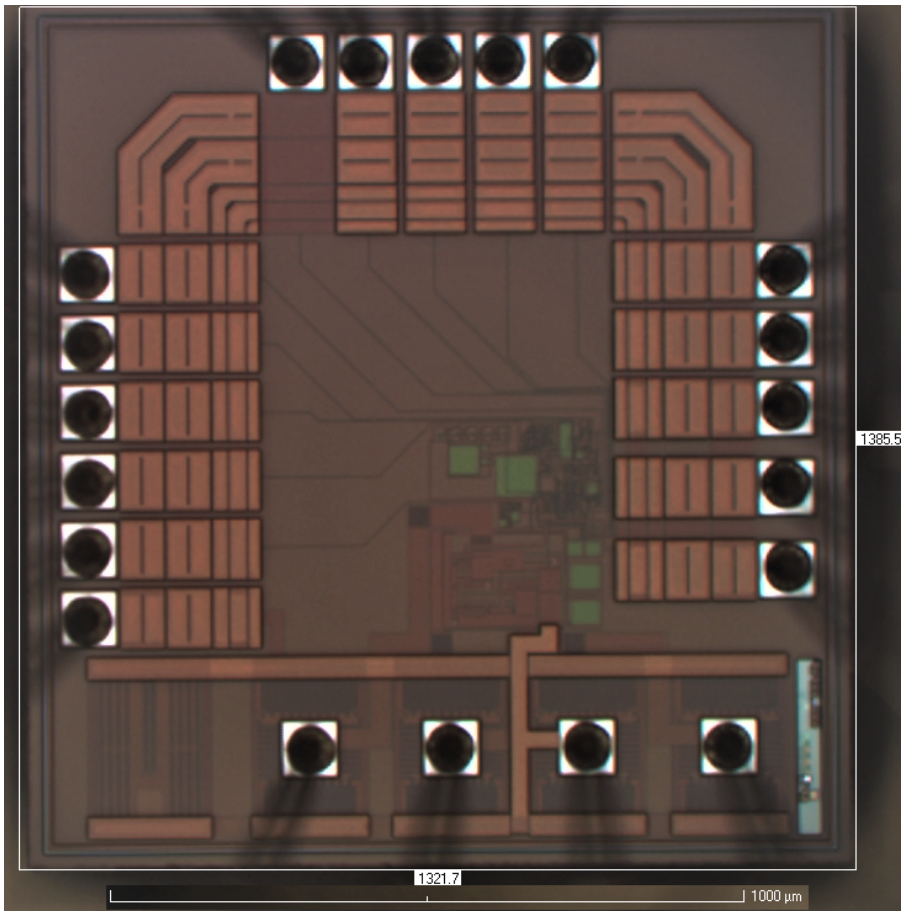

Figure 4.44: Micro photograph of the fabricated integrated circuit.

4.3.1 Integrated 15 Hz Oscillator and 200 kHz Sawtooth Generator

Measured results obtained while testing the 15 Hz oscillator are shown in Figure 4.45. A clock pulse is applied to the sample and hold circuit to store the current output voltage and after a short delay, a clock pulse is applied to the clocked comparator to compare the current output voltage to the previous output voltage. The measured frequency of the oscillator is 16.6 Hz, which is within the standard deviation of 6 Hz obtained in the Monte Carlo simulations [13]. The MPPT is still

able to work at this clocking frequency. The output of the sawtooth generator is shown in Figure 4.21, which is oscillating at a frequency of 217 kHz. This frequency is also within the standard deviation of 34 kHz obtained in the Monte Carlo simulations [13].

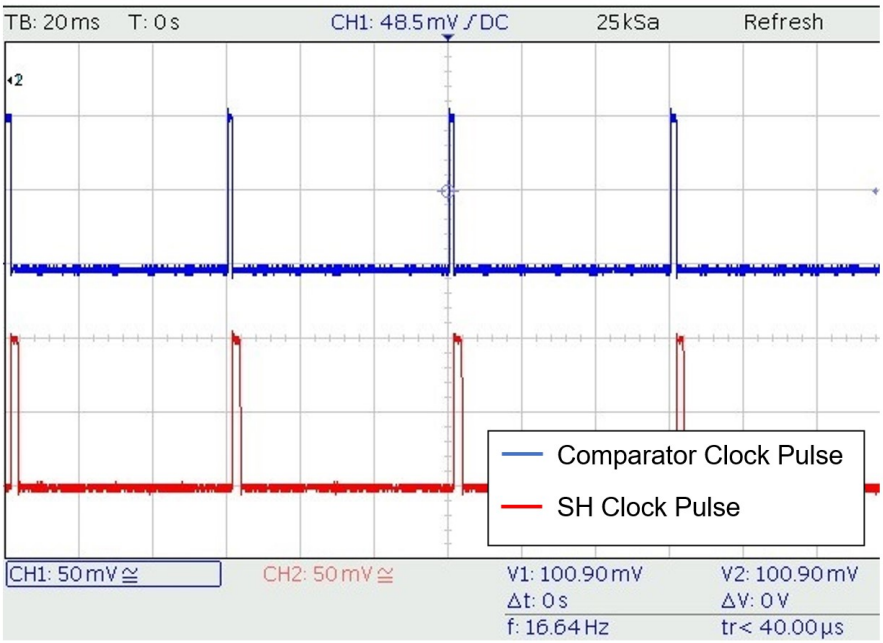

Figure 4.45: Comparator (blue) and sample and hold (red) clock pulses generated by the 15 Hz oscillator.

Figure 4.46: Measured results of the sawtooth signal generator.

4.3.2 Integrated Improved Dual Boost Converter

The improved dual boost converter is integrated in the same chip except for an externally connected 1 mH inductor and an output storage capacitor of 200 pF. The values of these two components can be varied but simulations indicated that with this inductance and capacitance, the circuit operates as expected throughout the whole operating range it is designed for. Furthermore, the size of these two components is not too large for typical energy harvesting applications.

The improved dual boost converter was initially tested at various input voltage, output load and duty cycle conditions and the measured results are presented in Figure 4.47. The input and output voltages together with the input current were recorded using the Keithley 2001 Precision Multimeter, which has a resolution of 10 pA [103]. The output current was calculated from the output voltage and the load resistance. A peak efficiency of 63.4% was measured with the boost converter in operation and a peak efficiency of 95.2% when operated just as a rectifier. A maximum voltage boosting ratio of 570% was obtained at continuous conduction mode (CCM) operation. A higher boosting ratio is achieved at discontinuous conduction mode (DCM) operation when the load resistance is large.

	$V_{IN}(V)$	$V_O(V)$	Eff. (%)	P_{IN}	P_O	Technology
[104]	80p-p	N/A	61	10 µW -1mW	N/A	0.35 µm+ Discrete
[105]	0.35-1.2	2.7-4.5	41	30 µW	7.1 µW	Discrete
[106]	N/A	2.4	60	277 µW	165 µW	0.25 µm
[107]	0.125-0.4	0-2.5	13	N/A	40 µW	90nm
[108]	0.5-2.5	3	60	N/A	3.9mW	0.5 µm
This Work	±0.5-± 50	1-50	63	10 µW-200mW	1 µW -60mW	0.35 µm

Table 4.10: Comparison of the on-chip AC/DC-to-DC converter with the SOA.

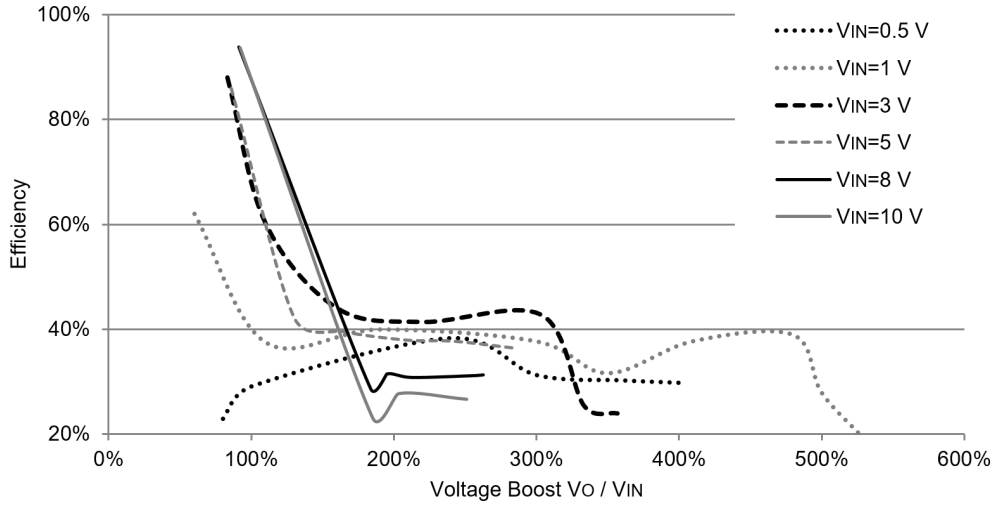

Figure 4.47: Measured results of the AC/DC-to-DC converter operated in CCM with 215 kΩ load resistance at various input voltage and duty cycle conditions.

Table 4.10 compares the measured performance of the converter designed within the proposed architecture with the state-of-the-art (SOA) of AC-DC converters designed for energy harvesters. The efficiency levels obtained compare with those of other converters but the input voltage and power range of the proposed converter is wider and so it can be used with a vaster range of energy harvesters. The circuit presented in [104] has a wide input voltage range of up to ±40 V, but this converter is not integrated since its transistors and passive components are all externally connected.

It is possible to further improve the converter to obtain a better conversion efficiency. One improvement is to increase the sizes of the high voltage transistors in the switch mode converter so that a higher current capability and better conversion efficiency. However, this would lower the efficiency at the lower end of the handling power due to higher switching losses. Another efficiency improvement could be obtained by paralleling of the pads and widening of track connections carrying the input and output currents of the converter. These improvements lower the conduction losses and as a result increase the conversion efficiency at the expense of more silicon area. Since the circuit's overall area is relatively small, it might be worthwhile compromising some additional area for a better efficiency output.

4.3.3 Testing of complete AC/DC-to-DC Converter and MPPT Function

Several minor changes were carried out in order for the MPPT to work reliably during the circuit characterisation. The MPPT clock frequency was slowed from 15 Hz to 10 Hz because in some cases, the changing duty cycle required a longer time for the boost converter to respond. This change eventually resulted in requiring a slower charge pump. Originally, the charge pump had an on-chip capacitance of 1 pF which is charged or discharged at a constant current of 1 nA. The charge pump output transient response was slowed down by adding an additional 2 pF capacitor, which was connected off chip.

The MPPT circuit was tested at various operating conditions. This was done by varying the input voltage, the input series resistance and the output load resistance at every test. The output voltage, the charge pump voltage and the toggle flip flop state were continuously monitored at a sampling rate of 1 ms. Fig. 4.48 shows how the MPPT circuit behaves when matching an output load of 90 kΩ to an input series resistance of 1 kΩ, operated with an input voltage of 5 V. The MPPT settling time was 22 s and the output voltage settled at 11.5 V. When the input

and output resistance were matched perfectly by the MPPT, the voltage across the internal resistance was equal to the voltage across the converter. During this test, at maximum power point, the voltage across the series resistance was measured at 1.5 V, meaning that the converter's input voltage was 3.5 V. It can be deduced that the MPPT could generate a higher output power by maintaining a higher voltage across the converter and the reason being that at a lower voltage, the converter's efficiency drops. The input power of the converter was 5.25 mW whereas its output power was 1.5 mW. The boost converter manages to boost the voltage by a factor of 3.25 at an efficiency of 24%. On the other hand, the MPPT's efficiency was measured at 99.96% when steady state was reached.

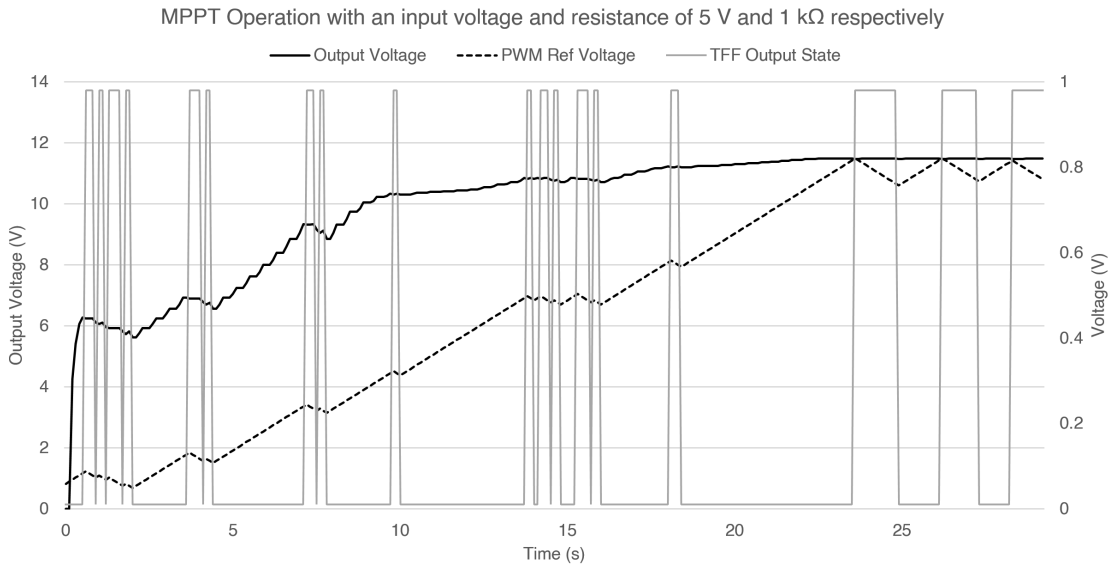

Figure 4.48: MPPT operation of the fabricated prototype at an input voltage of 5 V, an input resistance of 1 kΩ and output load of 90 kΩ.

Figure 4.49 shows how the MPPT circuit behaved when matching an output load of 90 kΩ to an input series resistance of 4.7 kΩ when operated with an input voltage of 2 V. The MPPT settling time was 8 s and the output voltage settled at 3.3 V. During this test, at maximum power point, the voltage across the series resistance was measured at 0.9 V which means that the converter's input voltage

was 1.1 V. Same as in the previous result, the MPPT obtained more power output by maintaining a slightly higher voltage across the converter. The input power of the converter is 191 µW whereas its output power is 121 µW. The efficiency of the converter is 63.4%. The MPPT's efficiency was measured at 99.90% due to a drop in the output voltage to 3.25 V between the toggled states of the flip flop.

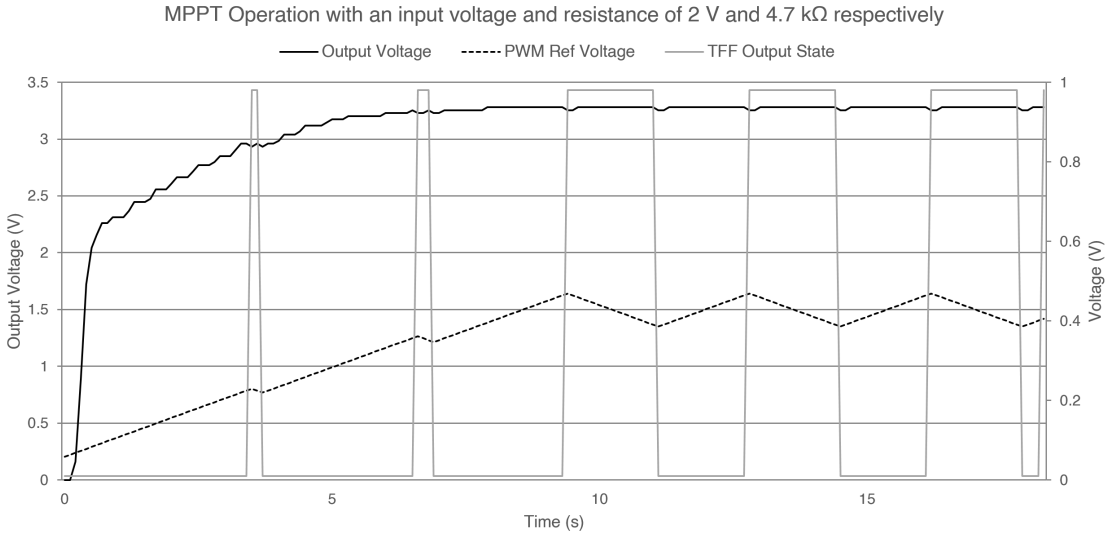

Figure 4.49: MPPT operation of the fabricated prototype at an input voltage of 2 V, an input resistance of 4.7 kΩ and an output load of 90 kΩ.

Figure 4.50 shows how the MPPT circuit behaved when matching an output load of 90 kΩ to an input series resistance of 2.2 kΩ when operated with an input voltage of 10 V. The MPPT settling time was 7.9 s and the output voltage settled at 15.93 V. During this test, at maximum power point, the voltage across the series resistance was measured at 2.7 V which means that the converter's input voltage was 7.3 V. The MPPT obtained more power output by maintaining a higher voltage across the converter. The input power of the converter is 8.96 mW whereas its output power is 2.82 mW. The efficiency of the converter is 31.5%. The MPPT's efficiency was measured at 99.86% due to a drop in the output voltage to 15.87 V between the toggled states of the flip flop.

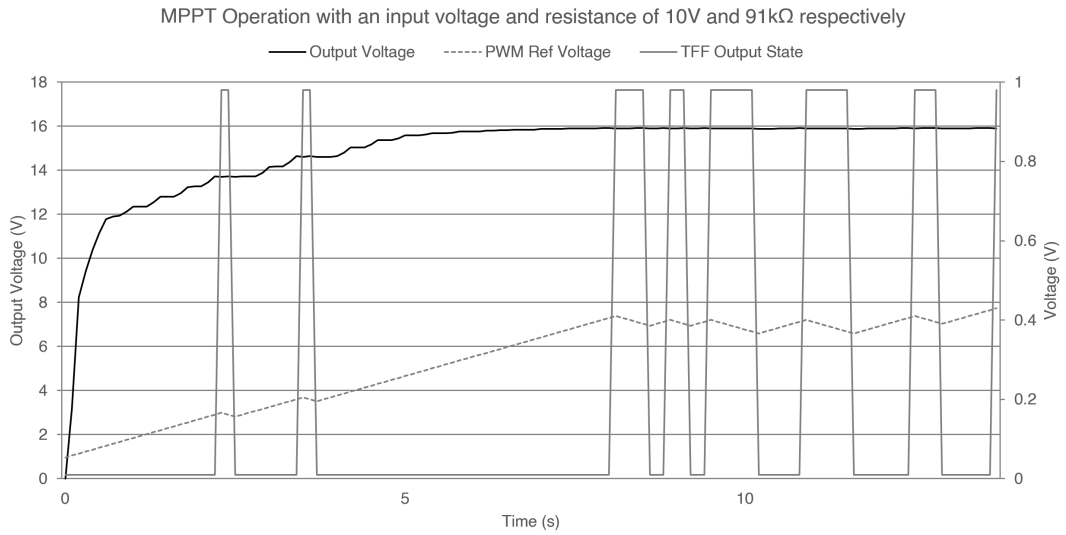

Figure 4.50: MPPT operation of the fabricated prototype at an input voltage of 10 V, an input resistance of 2.2 kΩ and an output load of 90 kΩ.

Figure 4.51 shows the measured input AC voltages before and after the input resistance of 1 kΩ when the circuit is being tested with a peak input voltage of 1.75 V at a frequency of 1 kHz. The output DC voltage reached 4 V across an output load of 64 kΩ.

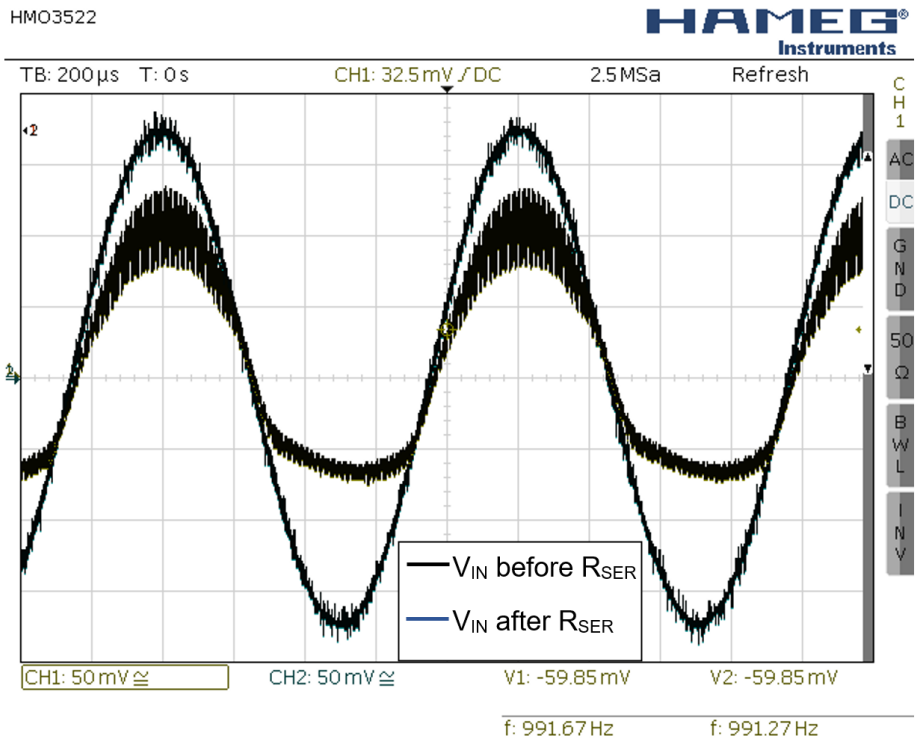

Figure 4.51: Input voltage measured before and after the input resistance during the MPPT operation at a peak AC input voltage of 1.75 V, 1 kHz.

The MPPT circuit was also tested with a 5 V 1.5 W solar cell under indoor light conditions. The open circuit voltage and short circuit current of this solar cell were 5.6 V and 1.7 mA respectively under this light condition. The results obtained when connecting the MPPT circuit to this solar cell are shown in Figure 4.52. This test shows that an output power of 3.1 mW was being generated by the MPPT circuit.

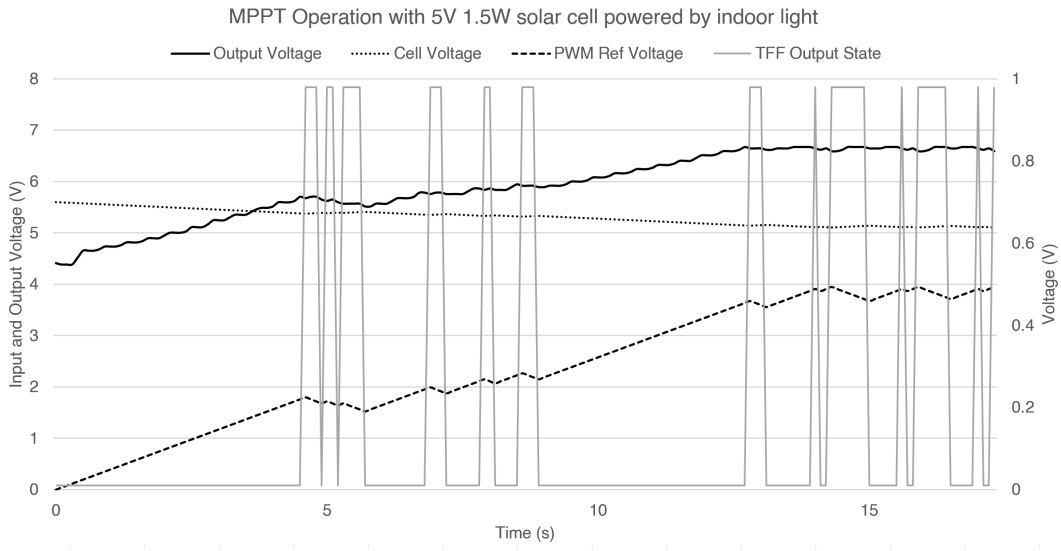

Figure 4.52: MPPT operation of the fabricated prototype connected to a 5 V solar cell and an output load of 10 kΩ.

The testing of the power conditioning circuit with a Mide PPA-1001 piezoelectric energy harvester was also carried out by means of a low force shaker at a vibrational rate of 400 Hz. The no load peak voltage generated by the energy harvester is 3.9 V as shown in Figure 4.53. The power conditioning circuit generated a DC output voltage of 4.1 V at a load of 10 kΩ as shown in Figure 4.54. This equates to a power of 1.7 mW.

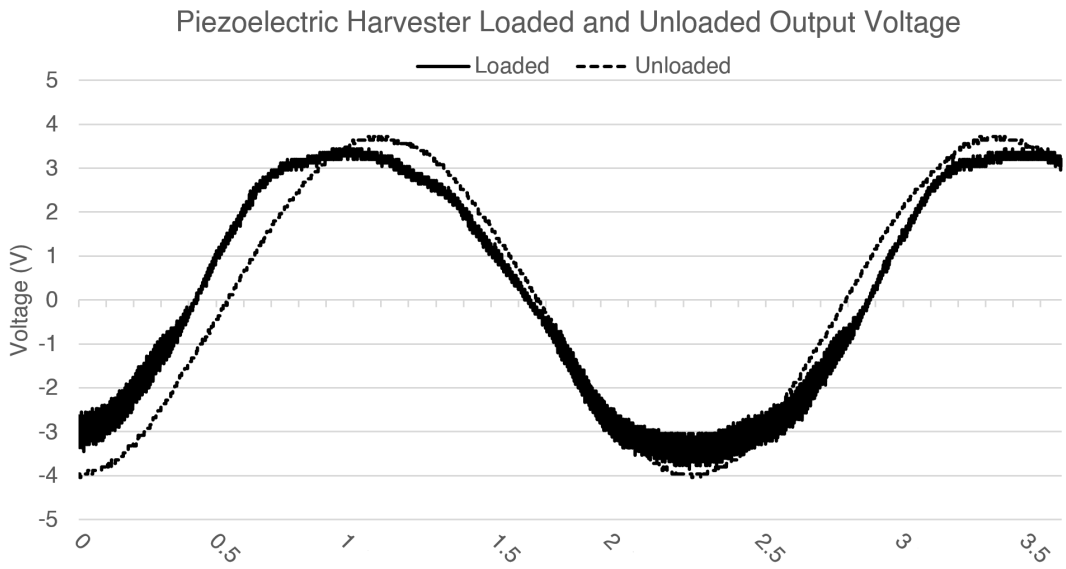

Figure 4.53: Piezoelectric energy harvester loaded and unloaded output voltage curves superimposed on same graph.

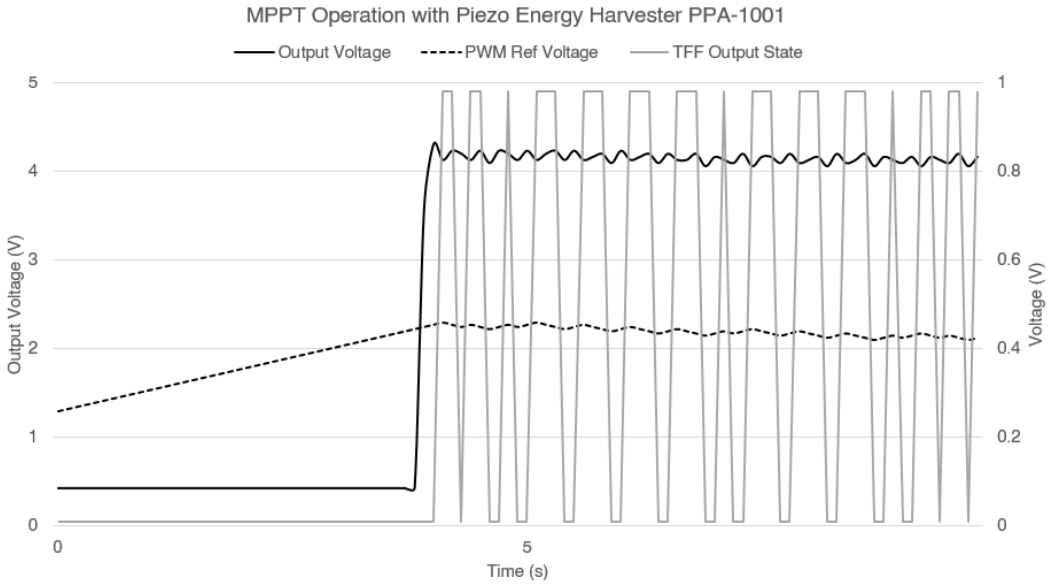

Figure 4.54: MPPT operation of the fabricated prototype connected to a piezoelectric energy harvester.

The integrated circuit was tested over a wide range of input voltages, input resistance and output load. Plots of these tests including the boost conversion

efficiency, the MPPT efficiency, input power and output power against input voltage are shown in Figure 4.55. The MPPT efficiency exceeded 99% in all tests. Conversion efficiency reached a maximum of 61% mainly because of the inefficiencies incurred by the integrated AC/DC-to-DC dual boost converter.

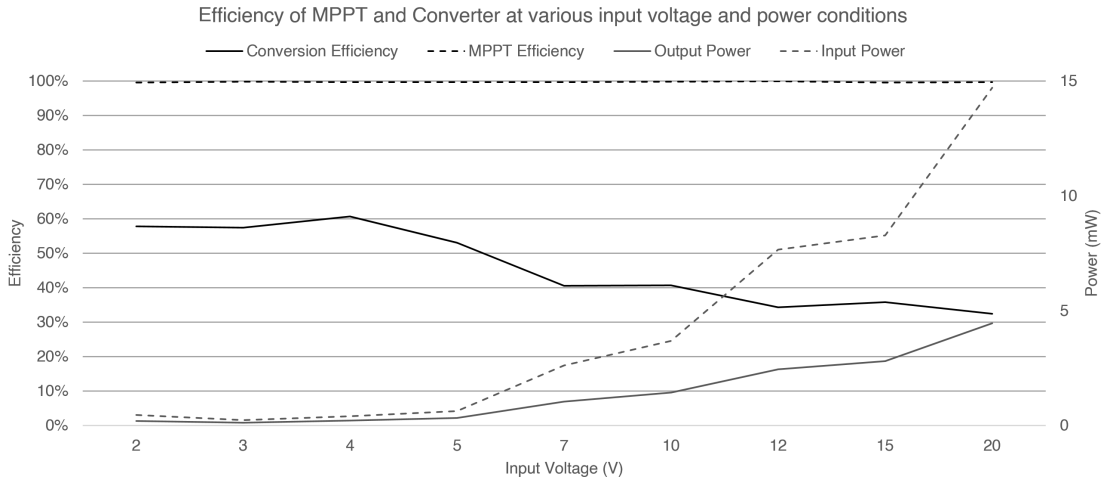

Figure 4.55: Measured efficiency of the MPPT and the AC/DC-to-DC converter of the fabricated prototype at various input voltage and power conditions.

Table 4.11 compares the performance of the proposed circuit with that of other designs reported in literature. The circuit designed and proposed in this work has the widest input and output voltage and power range and works with both AC and DC input voltages. Nonetheless, the efficiency levels are very similar to that of the SOA, while using either a similar or even cheaper fabrication technology. The design and fabrication of the voltage regulating DC-DC converter will be discussed in Chapter 5. This is to be connected to the output of the AC/DC-to-DC converter with MPPT control, in order to generate a constant output voltage and generate the voltage supply for the control circuitry. The converter efficiency was compared to the state of the art in [109].

Table 4.11: Comparison of the on-chip MPPT with the SOA.

	V_{IN}	V_O	MPPT Eff.	P_{IN}	P_O	Technology
[10]	0.21-0.65 VDC	0.6-1.8V	95.7-99.8%	N/A	1mW	0.18 µm
[110]	1.8-6.5 VAC	N/A	95.6%	N/A	254 µW	0.35 µm
[62]	5-60 VAC	2-5V	<99.9%	25 µW -1.6mW	N/A	0.25 µm +discrete
[111]	1.5-5 VDC	0-4V	99%	800 µW	N/A	0.35 µm
This Work	0.5-50 VAC/DC	1-50V	>99%	10 µW-200mW	1 µW -60mW	0.35 µm

4.4 Conclusion

The measured results of the complete AC/DC-to-DC converter with MPPT algorithm show that the novel circuitry implemented in this power conditioning circuit works as predicted by the simulations [6, 13]. The MPPT circuit was also tested with actual energy harvesters which prove that the proposed architecture and MPPT algorithm is compatible with different energy harvesting types and models. The converter was tested with both AC and DC input voltages and no degradation in performance was noted when operating with an AC input voltage. If this circuit is fabricated without the testing pads, the power consumption is expected to be less than 2 µW. The MPPT operation of the power conditioning integrated circuit could maintain the output voltage within 99% of maximum power point in all the tests carried out. The integrated AC/DC-to-DC converter works as expected with a peak efficiency of 63% [109]. Possible improvements to obtain a better conversion efficiency such as increase the sizes of the high voltage transistors in the switch

mode converter, paralleling of pads and track widening of connections carrying the input and output currents of the converter are all possible improvements which lowers the conduction losses and as a result increase the conversion efficiency. Since the circuit's overall area is relatively small, depending on the final application, it might be worthwhile compromising some additional area for a better conversion efficiency.

5. Voltage Regulating Buck Converter

5.1 Design of the Voltage Regulating Buck Converter

Following the design, fabrication and testing of the AC/DC-to-DC converter with MPPT control presented in Chapter 4, this chapter reports the design, fabrication and testing of a regulating voltage block. The MPPT control circuit of the first stage works with two supply voltage levels, 1 V and 2 V respectively, whereas the regulator's control is designed to operate with a single supply voltage of 2 V. This means that the power conditioning circuit requires the use of three regulators as shown in Figure 5.1. The first two regulators generate the 1 V and 2 V supplies to power all the control circuits of the power conditioner and a third regulator to supply an output voltage as required by the load. Although the reference output voltages of these regulators are different, these regulators are based on the same identical circuit because the change in the reference output voltage can be set by the resistance in the feedback loop. Thus, the fabricated integrated circuit includes three identical regulators which can be tested, monitored, and operated separately. The only common pins are their 2 V supply voltage and their input supply because they are to be connected to a common potential, across the high storage capacitor,

being fed from the output of the first stage.

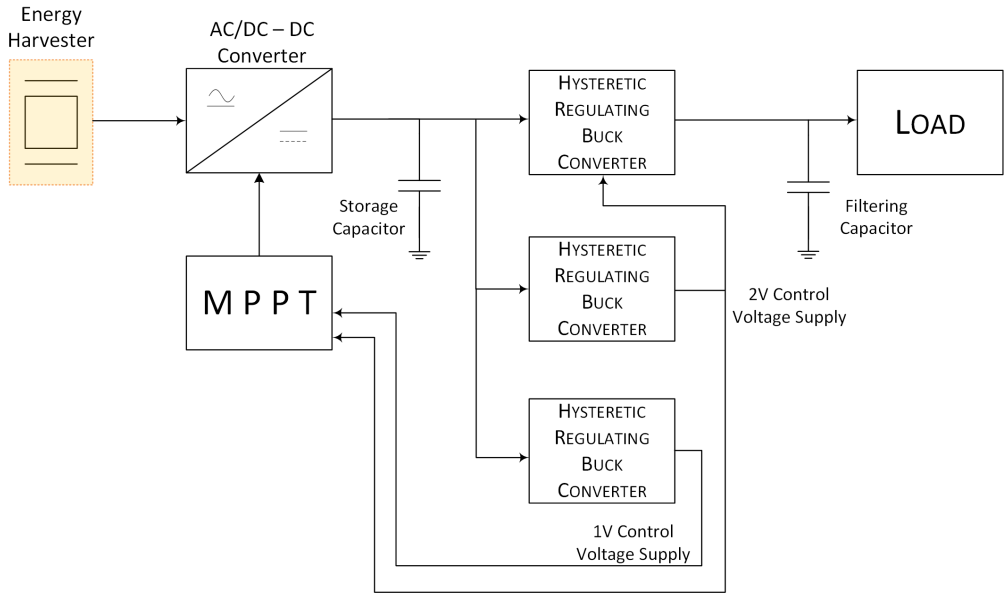

Figure 5.1: Block diagram of the proposed power conditioning circuit.

The proposed hysteretic controlled regulating buck converter consists of three main parts. A simplified schematic diagram of the complete circuit is shown in Figure 5.2. The first part is the low voltage stage which provides the hysteretic control and operates with a supply voltage of 2 V. This stage is capacitively coupled to the bootstrap gate drive circuit. These two stages are capacitively coupled since the second stage is a high voltage stage and so the capacitor acts as an isolation between these stages. In fact, the voltage swing of the capacitor's plate on the high voltage side varies at a high rate during switching and can reach up to 45 V with respect to ground. The final stage is the buck converter which steps down the input voltage, which may go up to 45 V, to the required output voltage.

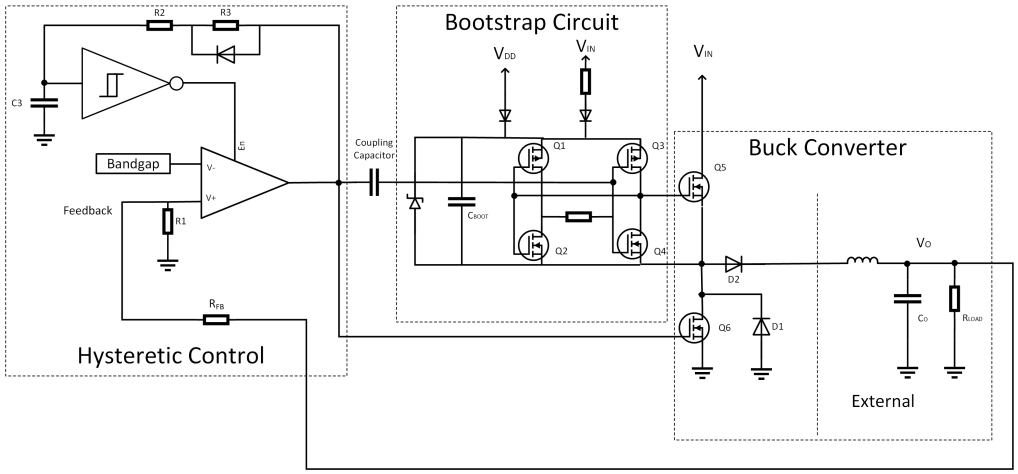

Figure 5.2: Simplified schematic diagram of the hysteretic controlled regulating Buck converter.

5.1.1 Hysteretic Control

The hysteretic control stage is shown in Figure 5.3. Control is achieved using a comparator. The comparator design is very similar to the circuit proposed in Section 4.1.5. As in the previous design, the transistors of the comparator are biased to operate in the sub-threshold region to maintain the power consumption to a minimum. The comparators are designed with a biasing current 5 nA. This biasing current is high enough for the comparator to drive its output inverter with an adequate slew rate of 10 V/µs. The inverter is designed to drive both the bootstrapping circuit through the coupling capacitor and the low side NMOS transistor paralleling the freewheeling diode. The bias current can be externally increased or decreased, so that the circuit can be tested at different bias currents.

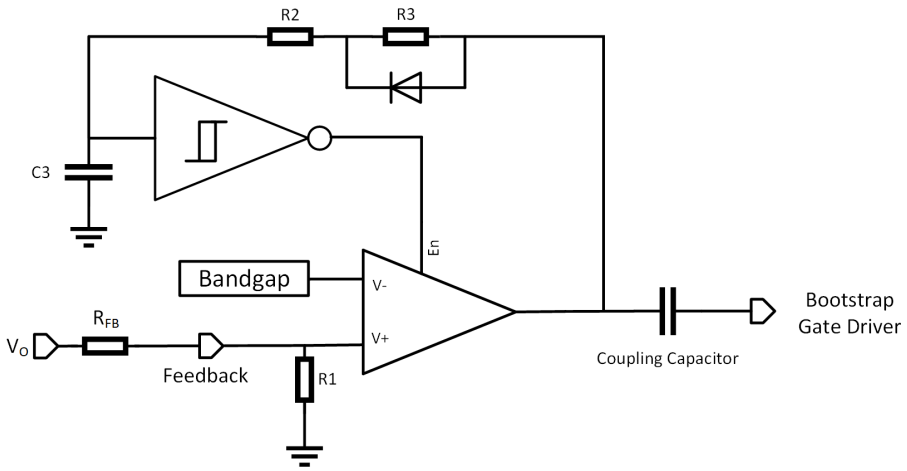

Figure 5.3: Circuit diagram of the hysteretic control stage.

The hysteresis element is not included in the comparator itself, but hysteresis still happens in the L-C components of the buck converter which are externally connected. Once the output voltage reaches the reference voltage and the comparator switches off the high side transistor of the buck converter, the energy stored in the inductor due to its forward current is transferred into the output capacitor. As a result, the voltage across the output capacitor exceeds the reference voltage. The reference output voltage of the regulator can be set externally through the sizing of a feedback resistor.

The comparator compares the output voltage fed back through the external feedback resistor R_{FB} with a reference voltage of 0.6 V generated via a bandgap circuit. The value of resistor R1 in Figure 5.3 is 50 kΩ. R1 is integrated and its resistance value is limited by the amount of chip area to be sacrificed. However, since the voltage across this resistor will be 0.6 V, the power dissipated across it will be 12 µW. The value of the feedback resistor in kΩ with respect to the required output voltage V_O is given by Eq. 5.2. The total power consumption across resistors R1 and R_{FB} is given by Eq. 5.3.

$$R_{FB} = \frac{R_1}{V^-}\left(V_O - V^-\right) \tag{5.1}$$

Substituting $V-$ with 0.6 V and R_1 with 50 kΩ in Eq. 5.1 gives;

$$R_{FB} = 83\left(V_O - 0.6\right) \tag{5.2}$$

$$P_{dis.} = \frac{V_O^2}{R_1 + R_{FB}} = \frac{V_O^2}{R_1 + 83V_O - 49.8} \approx \frac{V_O^2}{50\,\text{k}\Omega + 83V_O} \tag{5.3}$$

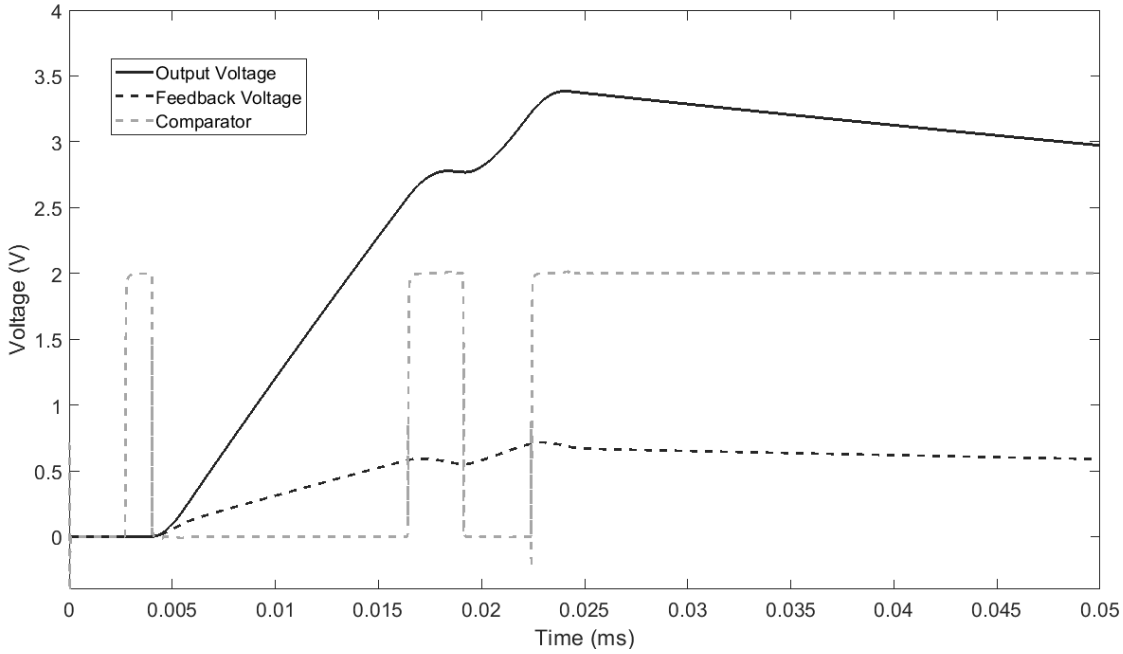

Figure 5.4: Derivative feedback is used to lower the voltage overshoot during the startup phase.

A disadvantage of hysteretic controlled converters is the voltage overshoot upon startup. This happens because the buck converter is switched off only once the voltage across the output capacitor reaches the reference voltage. At this point, the current in the inductor would have risen substantially and as a result the stored

energy of the inductor is quite high. All the inductor's energy is transferred to the output capacitor upon switching off the buck converter and leads to a voltage overshoot on the output capacitor. The correct sizing of the externally connected inductor and output capacitor, depending on the converter's normal operating current and voltage can reach a balance between voltage overshoot at startup and output ripple voltage. Additionally, a capacitor can be connected in parallel with the feedback resistor to obtain a proportional-derivative control element in order to lower the voltage overshoot during startup and the output ripple voltages as shown in Figure 5.4. This switches off the comparator slightly before the output voltage reaches the reference voltage.

A problem with bootstrapping circuits is the discharging of the bootstrap capacitor. In order not to allow the bootstrap capacitor to discharge and in turn ensure that the high side NMOS transistor keeps operating in the triode region, the control circuit is designed such that it temporarily disables the comparator after long on periods. The comparator's output goes high, making the bootstrap circuit switch off the buck converter for an adequate time until the bootstrap capacitor charges again. This is achieved by the Schmitt inverter which upon the discharge of capacitor C_3, disables the comparator temporarily until C_3 is charged up again as shown in Figure 5.5. The Schmitt inverter design is similar to the one designed in the MPPT in Section 4.1.1. The values of resistors R2 and R3 determine the duty cycle and the frequency of the enable pulses. Their sizes are set to disable the comparator for 1 µs after an on period of 13 µs. During startup, when the on period exceeds 13 µs, the Schmitt inverter temporarily disables the comparator and together with derivative feedback, lowers the startup voltage overshoot as seen in Figure 5.5.

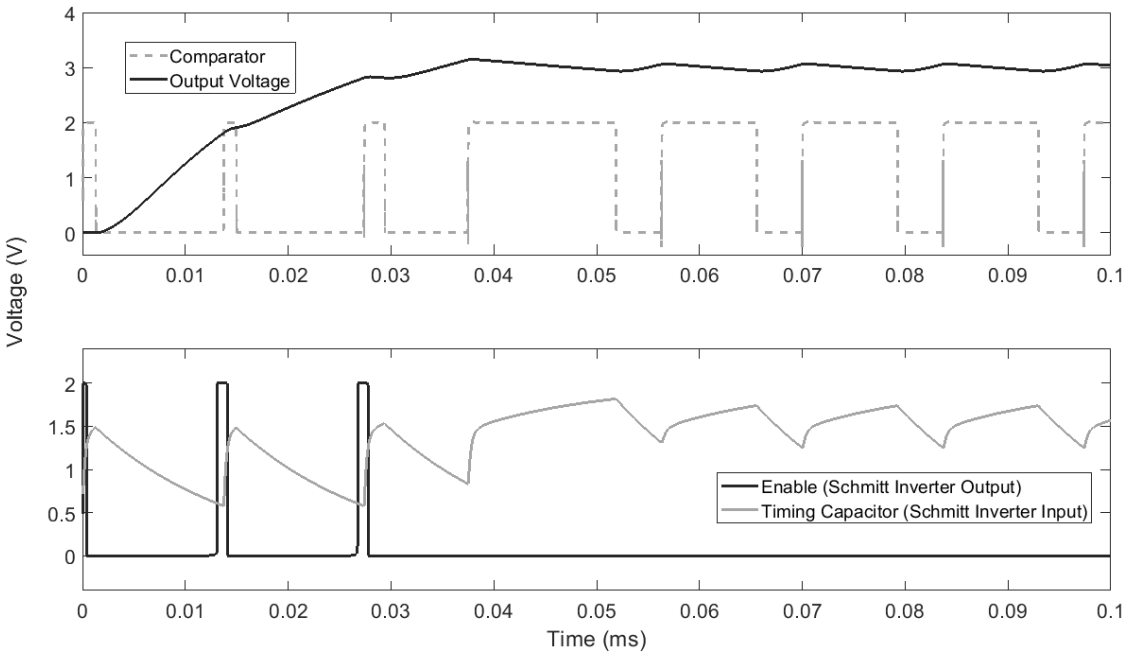

Figure 5.5: The comparator is periodically disabled in order to switch off the bootstrap circuit and recharge the capacitor C_{BOOT}.

5.1.2 Bootstrapping Circuit

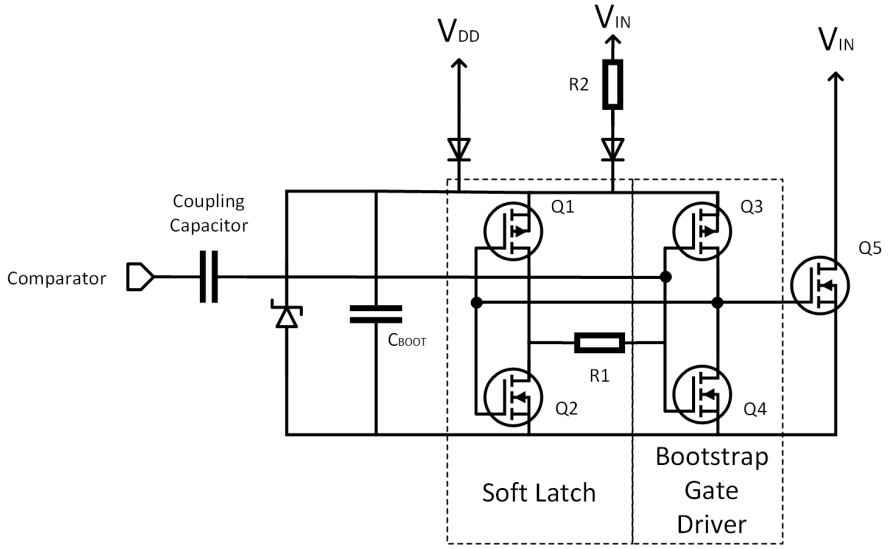

Figure 5.6: Simplified diagram of the bootstrap gate drive circuit.

The bootstrap gate drive circuit is shown in Figure 5.6. The coupling capacitor is implemented on chip as well and its capacitance is 6.2 pF. The coupling capacitor is driven by the comparator from the previous stage. V_{DD} is the supply voltage of 2 V whereas V_{IN} is the input voltage which can range from 1.5 V to 45 V. The C_{BOOT} capacitor charges from whichever voltage is highest and its voltage is clamped to 3 V because the absolute maximum V_{GS} voltage on the high side NMOS transistor is 3.3 V. Maximum operating efficiency of the converter is achieved when V_{IN} is 3.7 V or higher, because after taking in consideration the diode forward voltage drop, the voltage across C_{BOOT} would have reached 3 V.

When the comparator pulls down its output from 2 V to 0 V, the gate driving stage charges the high side NMOS gate capacitance of transistor $Q5$. This is done through transistor $Q3$, using the stored charge of capacitor C_{BOOT}. As the source of transistor $Q5$ increases towards V_{IN}, the gates of transistors $Q3$ and $Q4$ are pulled further down by the coupling capacitor, thus creating an indirect positive feedback latching mechanism. This ensures that the state is changed and maintained until $Q5$ fully switches on to the triode region. Effectively the bootstrapping circuit is sensitive to the differentiation (pull up or pull down) of the coupling capacitor voltage. An additional soft latch is implemented in the circuit via transistors $Q1$ and $Q2$ and resistor R_1. This ensures that the state is latched until the comparator changes its output back to 2 V. A simulation of the bootstrap circuit is shown in Figure 5.7 with the regulating buck converter maintaining a 3 V output voltage.

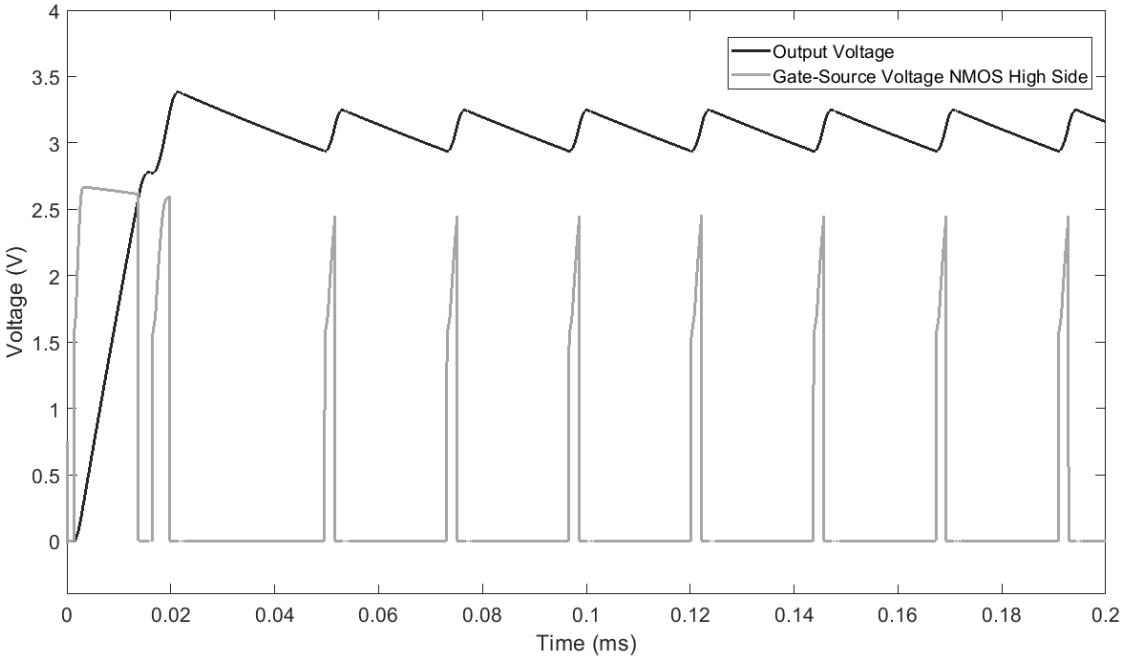

Figure 5.7: Gate-to-source voltage of the high side NMOS transistor of the buck converter which is generated by the bootstrap circuit.

5.1.3 Buck Converter

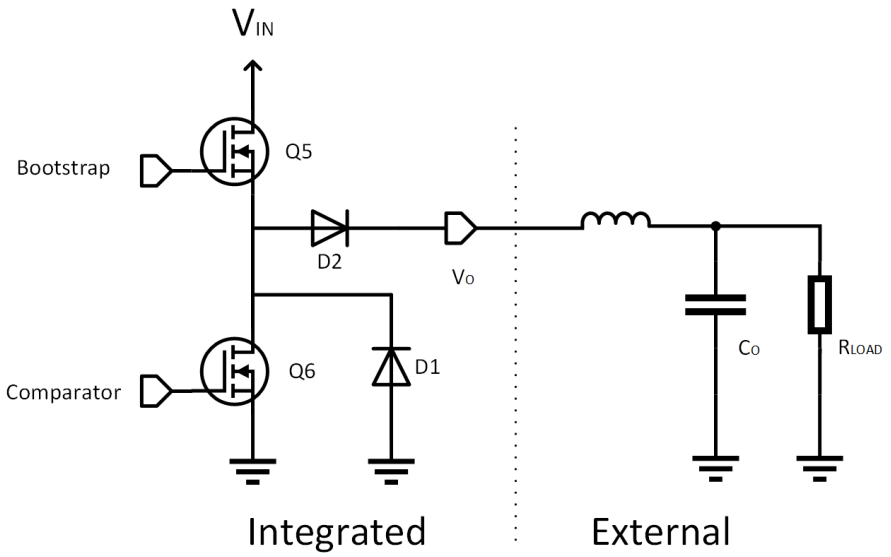

Figure 5.8: Schematic diagram of the regulating buck converter.

The buck converter implemented in this regulator is shown in Figure 5.8. The output inductor and capacitor are not integrated and must be externally connected. They can be sized specifically according to the voltage, current and ripple requirements. The feedback is taken from the voltage across capacitor C_O. Diode D1 is the freewheeling diode of the buck converter and most of its current is conducted by transistor $Q6$. This achieves a higher conversion efficiency because transistor $Q6$ has a lower voltage drop than diode D1.

The ideal buck converter transfer function operating in CCM is given by Eq. 5.4. Eq. 5.13 denotes the duty cycle when considering the conduction losses of the diode, switching devices and inductor. Eq. 5.16 determines the efficiency of the buck converter from Eq. 5.13.

$$D = \frac{V_O}{V_{IN}} \tag{5.4}$$

$$\delta I_{L_{ON}} + \delta I_{L_{OFF}} = 0 \tag{5.5}$$

$$V_L = L\frac{\delta I_L}{\delta t} \tag{5.6}$$

$$\delta I_L = \frac{\delta t}{L} V_L \tag{5.7}$$

Substituting Eq. 5.7 into Eq. 5.5;

$$\frac{DT}{L}\left(V_{IN} - V_O - V_L - V_D - V_{SW}\right) + \frac{\left(1-D\right)T}{L}\left(-V_L - V_{SY} - V_O - V_D\right) = 0 \tag{5.8}$$

$$D\left(V_{IN} - V_O - V_L - V_D - V_{SW}\right) + \left(1-D\right)\left(-V_L - V_{SY} - V_O - V_D\right) = 0 \tag{5.9}$$

where D is the Duty Cycle, V_O is the output voltage, V_{IN} is the input voltage, V_{SY} is the voltage across the synchronous transistor $Q6$, V_L is the inductor voltage

drop, and V_{SW} is the voltage across the switching device $Q5$.

$$\begin{aligned} DV_{IN} - DV_O - DV_L - DV_D - DV_{SW} + DV_L + DV_{SY} \\ +DV_O + DV_D - V_L - V_{SY} - V_O - V_D = 0 \end{aligned} \tag{5.10}$$

$$DV_{IN} - DV_{SW} + DV_{SY} - V_L - V_{SY} - V_O - V_D = 0 \tag{5.11}$$

$$D\left(V_{IN} - V_{SW} + V_{SY}\right) = V_L + V_{SY} + V_O + V_D \tag{5.12}$$

$$D = \frac{V_O + V_D + V_L + V_{SY}}{V_{IN} - V_{SW} + V_{SY}} \tag{5.13}$$

$$\eta = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_{IN} I_{IN}} \tag{5.14}$$

$$I_{IN} = DI_O \tag{5.15}$$

$$\eta = \frac{V_O}{V_{IN} D} \tag{5.16}$$

Diode D2 is essential when the buck converter operates in DCM because as soon as the inductor current drops to zero, the source voltage of the high side NMOS transistor $Q5$ increases to the voltage across capacitor C_O. As a result, the bootstrap circuit switches its state and turns on transistor $Q5$, since the bootstrap circuit senses a pull down from the coupling capacitor. This is shown in Figure 5.9. By including diode D2 in the buck converter, it is ensured that the bootstrap circuit never switches on $Q5$ as the inductor's current drops to zero. Diode D2 also prevents a negative current from flowing from capacitor C_O to $Q6$ during the switched off period, when the converter is operating in DCM.

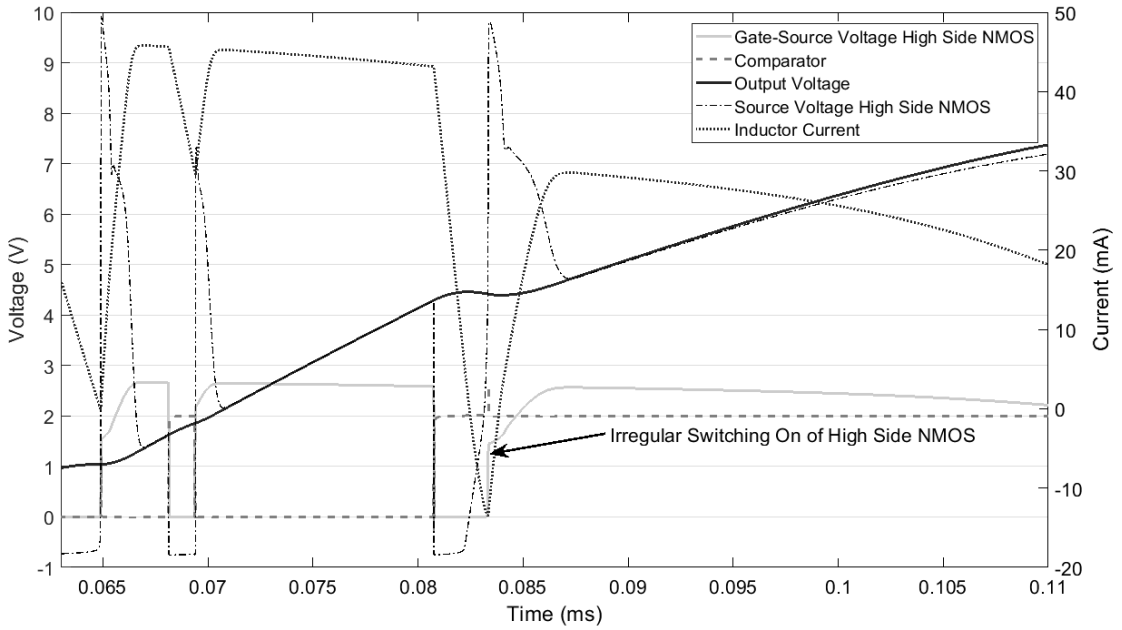

Figure 5.9: A simulation showing the unreliable operation of the bootstrap circuit without diode D2, where the output voltage keeps increasing due to incorrect switching.

5.2 Simulation Results

Simulations were carried out to assess the total power consumption and the functionality of the circuit blocks at various temperature and process conditions. Figure 5.10 shows the results of the simulation of the converter at an input voltage of 10 V, loaded with a 6 kΩ resistance and set to output a voltage of 3 V. The inductor and capacitor values in this simulation are 200 µH and 200 nF respectively. The inductor current of one on cycle is shown. The ripple output voltage in this simulation is 5% and the conversion efficiency is 71%. Additional simulations were carried out and data was analysed to determine the operating efficiency of the hysteretic buck converter at various operating conditions. The efficiency of the converter varies depending on several parameters like the output current, the input voltage and the output voltage. The peak conversion efficiency of the buck converter reaches 82% at an input voltage of 25 V, an output voltage of 5 V and

an output power of 2 mW whereas the control power consumption is 0.5 µW. The output voltage ripple is 2.3%.

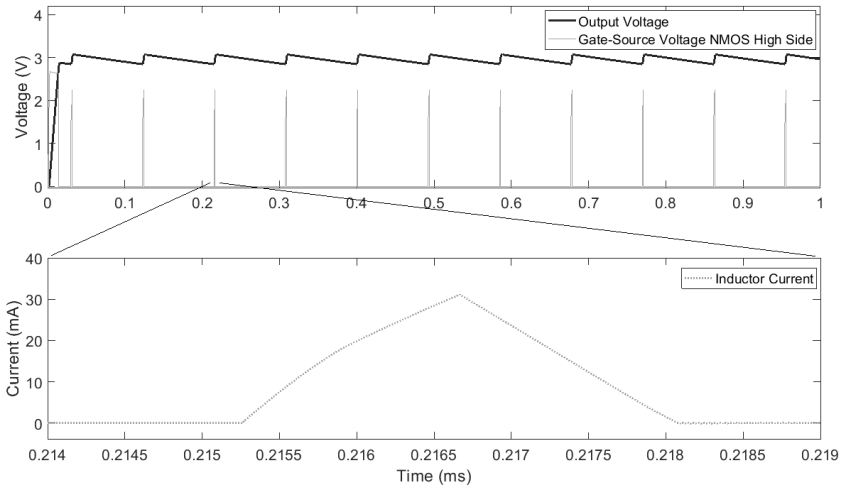

Figure 5.10: Simulation of the buck converter with an input voltage of 10 V, an output voltage of 3 V and an output load resistance of 6 kΩ.

5.3 Circuit Layout

Following the circuit design and simulations at various temperature, voltage and process conditions, the layout of the circuit was carried out. Particular attention was given to every component selected so that the absolute maximum voltage limit between the terminals of each component and between every terminal and substrate is not exceeded during the normal operation of the circuit. All the transistors, diodes and passive components in the bootstrap circuit and buck converter are isolated from the substrate due to the high voltages they are intended to experience.

Same as in the previous fabrication, a number of precautions were taken in the layout stage so that the circuit works as expected once it is fabricated. The layout shielded the noise generated by the high switching voltages in the bootstrap and buck converter so that it does not affect the hysteretic control part. This part of the circuit is very prone to noise due to its low bias currents. Apart from the

matching of transistors in current mirrors, and differential amplifiers, shielding and spacing are the precautions taken to reduce the noise generated in the hysteretic control circuitry. Another aspect which had to be considered in the layout design is the high currents and voltages involved in the power circuitry. High currents require sufficiently wide and thick metal interconnects so that no damage is done by the continuous current during normal operation and also to reduce the voltage drop across these metal interconnects. Furthermore, the metal interconnects are sufficiently spaced in order to take into account the high electric field requirement due to the high voltage requirements. The interconnects between the integrated part of the buck converter and the externally connected inductor and capacitor are externally connected were designed wide enough so that the combined inductance and resistance of the pads and metal interconnects in between do not create voltage overshoots due to the switch on and switch off delays of the transistors. Furthermore, in the bonding of the integrated circuit with the package, two pins were connected to every high voltage pad as shown in Figure 5.11. This further reduces the impedance from the integrated circuit towards the externally connected components.

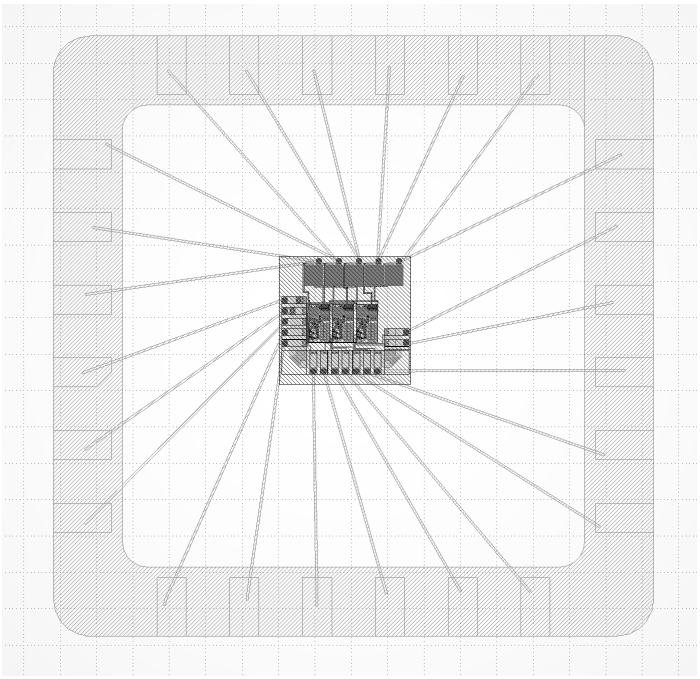

Figure 5.11: Layout of the hysteretically controlled regulating buck converter.

The layout of the hysteretic buck regulator is shown in Figure 5.12, with all the respective components adequately labelled. Pads were included at the input and output of every block, so that each individual block could be monitored externally and maximize its testability. The dimensions of one hysteretic converter without pads is 530 µm by 284 µm, that is an area of 0.15 mm^2. The fabricated integrated circuit contains three copies of the same converter. The total dimensions of the three converters and pads is 1.6 mm by 1.8 mm, that is an area of 2.9 mm^2. The layout includes five high voltage pads and fourteen low voltage pads as shown in Figure 5.13.

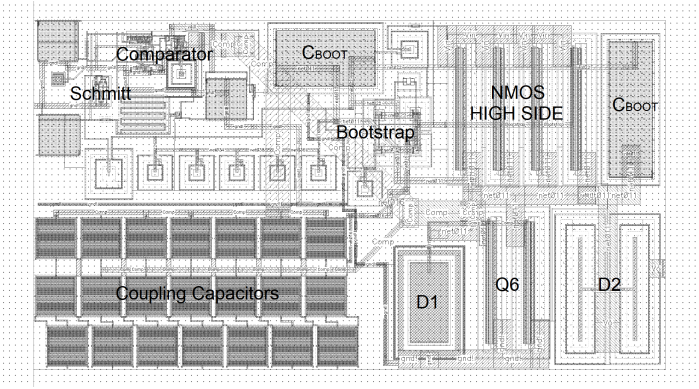

Figure 5.12: Layout of the hysteretically controlled regulating buck converter.

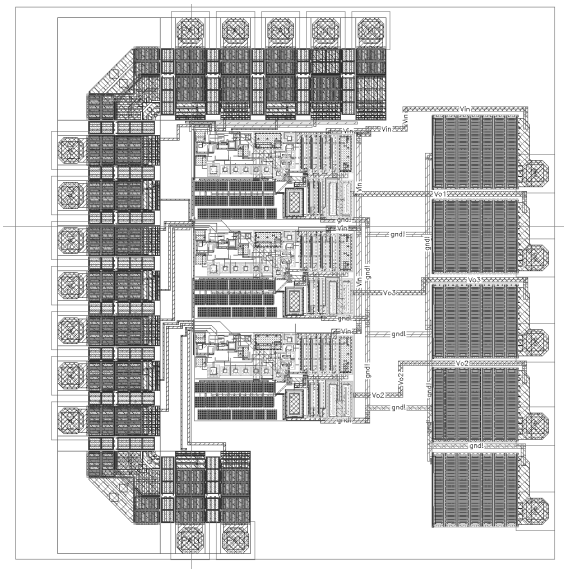

Figure 5.13: Layout of the integrated circuit with the three regulators including all their respective pads.

One of the three converters is capable to generate the 2 V supply voltage (V_{DD}) required for all the three converters to operate. Cold starting the converter supplying V_{DD} can be achieved externally by connecting an additional capacitor from the input voltage V_{IN} to the output of this converter (which in this case also must be connected to V_{DD}) so that as soon as a voltage is applied on the input of the converters, a temporary voltage supply is generated on the comparator to startup the converters.

5.4 Post Layout Simulation Results

Post layout simulations were carried out prior to sending the design for fabrication to ensure that all circuitry behaves as expected even when considering the parasitic capacitances and resistances of the interconnections. Quantus was used to extract the parasitic capacitances of the circuits and then the derived model is used by Analog Design Environments (ADE) software to carry out the post layout simulations. The converters were tested at various input and output voltage conditions to ensure correct performance throughout. When comparing normal simulations with post layout simulations a negligible increase in the output ripple voltage could be noted due to a marginal slower response by the comparator when considering the parasitic capacitances. This was not of a concern especially since the ripple voltage can be reduced by varying the size of the external inductor and capacitor. The first post layout simulation was carried out with the regulator operating at an input and output voltage of 10 V and 1 V respectively, an output load of 500 Ω, output inductor of 80 µH and an output capacitor of 300 nF. The value of the feedback capacitor was set to 1 pF to lower the voltage overshoot. Figure 5.14 plots the comparator output, the gate voltage of the buck converter high side transistor generated by the bootstrapping circuit and the output voltage. The average output voltage measured 1.03 V, the overshoot voltage reached 1.58 V and then ranged from 0.77 V to 1.31 V, that is percentage ripple voltage of 26 %. When the regulator is set to output such a low output voltage, the percentage ripple voltages may be substantial, and an additional L-C filter may be required to lower the ripple voltages in supply voltage sensitive applications.

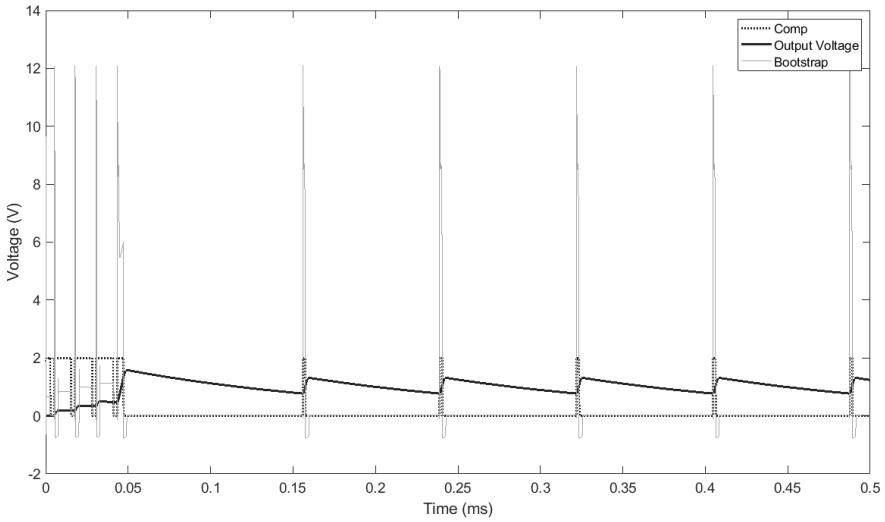

Figure 5.14: Simulation of the buck converter with an input voltage of 10 V, output voltage set to 1 V and an output load resistance of 500 Ω.

The second post layout simulation was carried out with the regulator's input voltage increased to 20 V, while maintaining all the components sizes to the same values. Figure 5.15 plots the comparator output and the output voltage. The average output voltage measures 1.00 V, the overshoot voltage reached 1.15 V and then ranged from 0.932 V to 1.05 V, that is a percentage ripple voltage of 5.9 %.

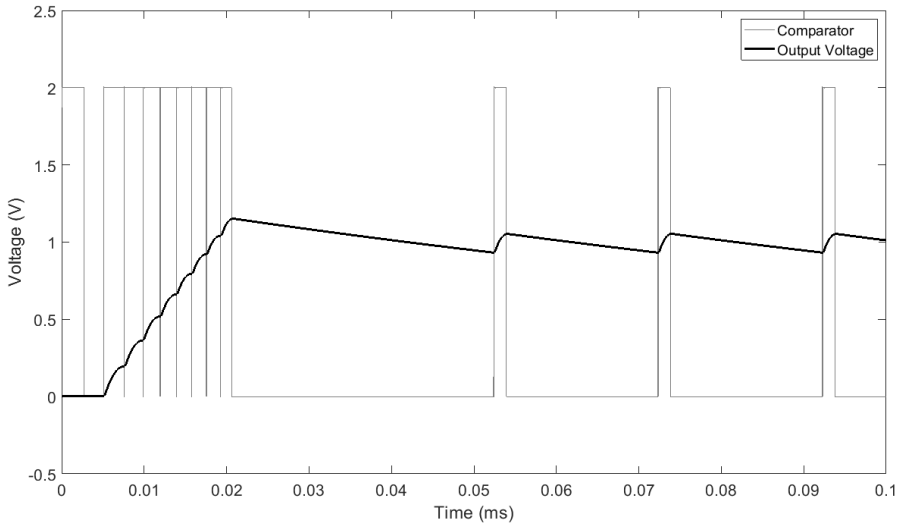

Figure 5.15: Simulation of the buck converter with an input voltage of 20 V, output voltage set to 1 V and an output load resistance of 500 Ω.

Another simulation was carried out at a higher input voltage of 30 V but maintaining same component values. Figure 5.16 plots the comparator and output voltage obtained from this simulation. The average output voltage measured 1.03 V, the overshoot voltage reached 1.08 V and then ranged from 0.932 V to 1.05 V, that is a percentage ripple voltage of 7.1 %.

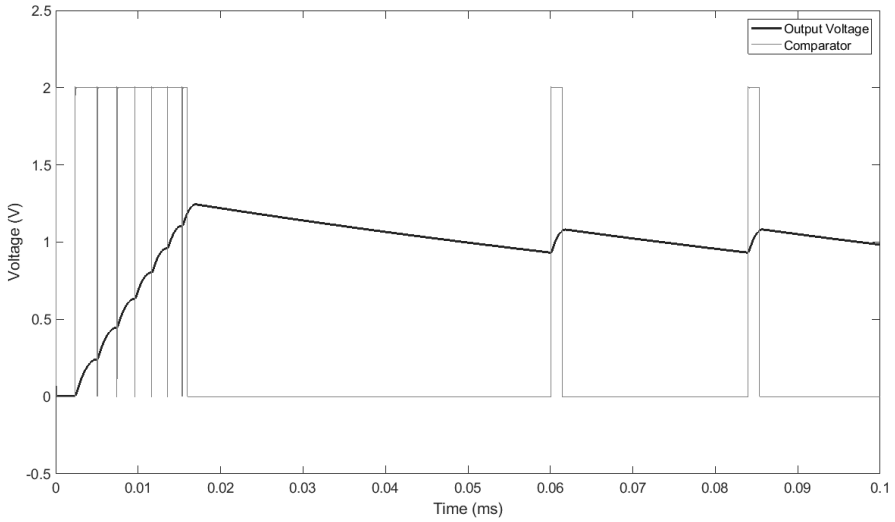

Figure 5.16: Simulation of the buck converter with an input voltage of 30 V, output voltage set to 1 V and an output load resistance of 500 Ω.

Figure 5.17 shows the simulation results when the regulator was simulated at an input voltage of 40 V. The average output voltage measured 1.04 V, the overshoot voltage reached 1.33 V and then ranged from 0.932 V to 1.12 V, that is a percentage ripple voltage of 9 %.

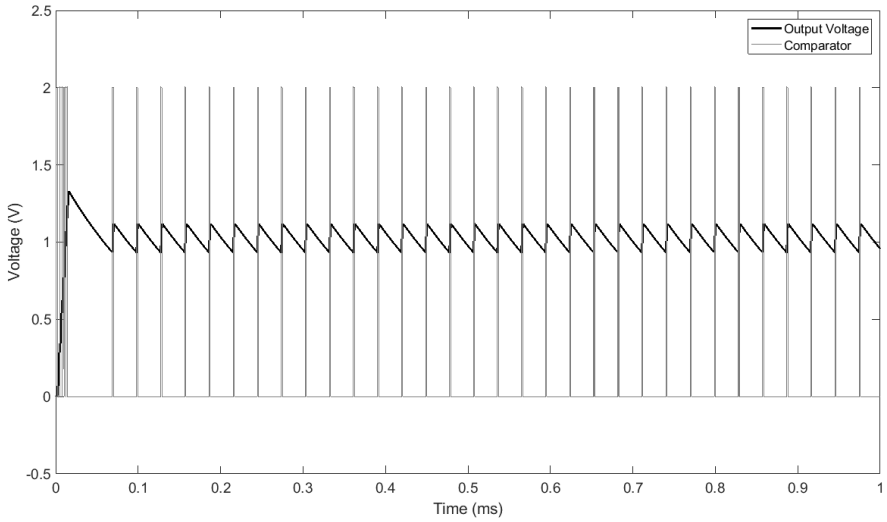

Figure 5.17: Simulation of the buck converter with an input voltage of 40 V, output voltage set to 1 V and an output load resistance of 500 Ω.

The value of the feedback resistor was increased so that the output voltage of the regulator is set to 2 V. The output load was increased to 2 kΩ, maintaining the same output power. The inductance of the output inductor is set to 100 µH and the capacitance of the output capacitor is set to 200 nF and the feedback capacitor is set to 20 pF to increase the derivative element to further limit the startup voltage overshoot. Figure 5.18 plots the comparator output, the gate voltage of the buck converter high side transistor generated by the bootstrapping circuit and the output voltage. The average output voltage measures 1.97 V, the overshoot voltage reached 2.59 V and then ranged from 1.69 V to 2.18 V, that is percentage ripple voltage of 12 %.

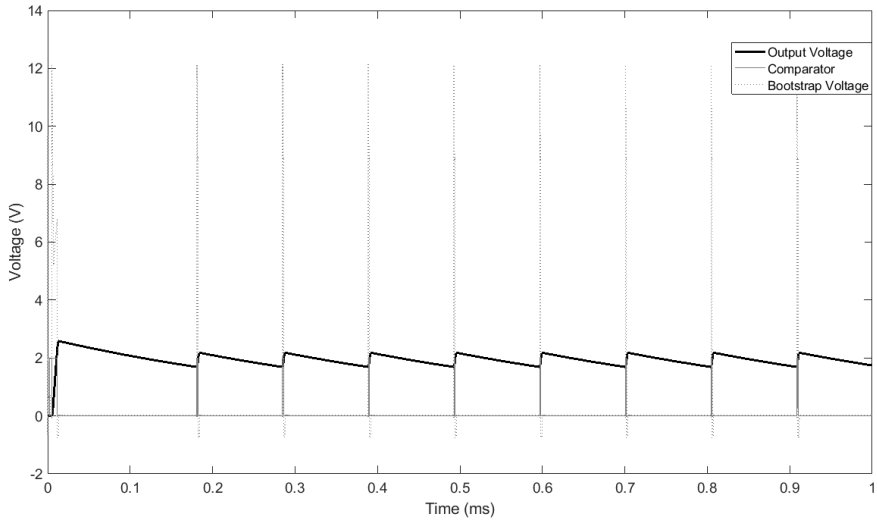

Figure 5.18: Simulation of the buck converter with an input voltage of 10 V, output voltage set to 2 V and an output load resistance of 2 kΩ.

Increasing the input voltage to 20 V but maintaining the same component values yields the output graphs shown in Figure 5.19. The measured average output voltage is 2.00 V, the overshoot voltage reached 2.11 V and then ranged from 1.89 V to 2.08 V, that is percentage ripple voltage of 4.8 %.

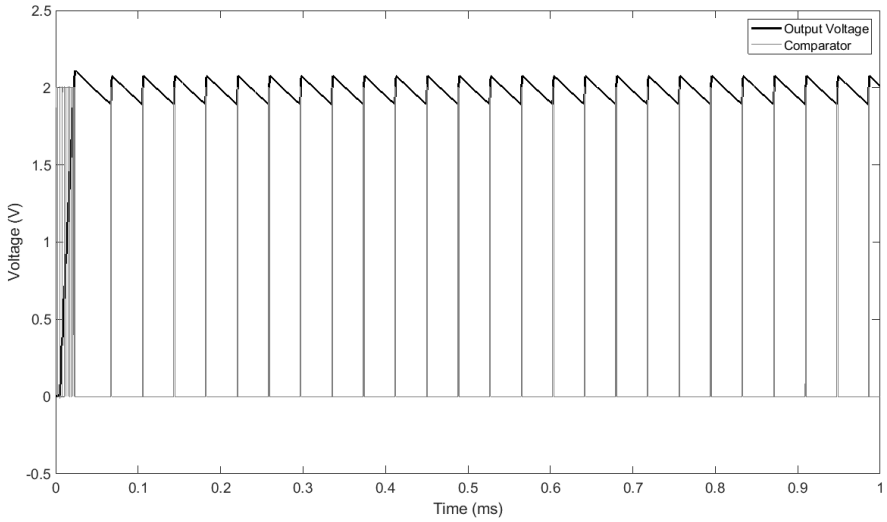

Figure 5.19: Simulation of the buck converter with an input voltage of 20 V, output voltage set to 2 V and an output load resistance of 2 kΩ.

Operating the regulator at an input voltage of 30 V and maintaining same component parameters, gives the outputs plotted in Figure 5.20. The average output voltage throughout the simulation is 2.02 V and the overshoot voltage during startup reached 2.19 V. After startup the output voltage ranged from 1.89 V to 2.10 V. The percentage ripple voltage in this simulation resulted to 5.3 %.

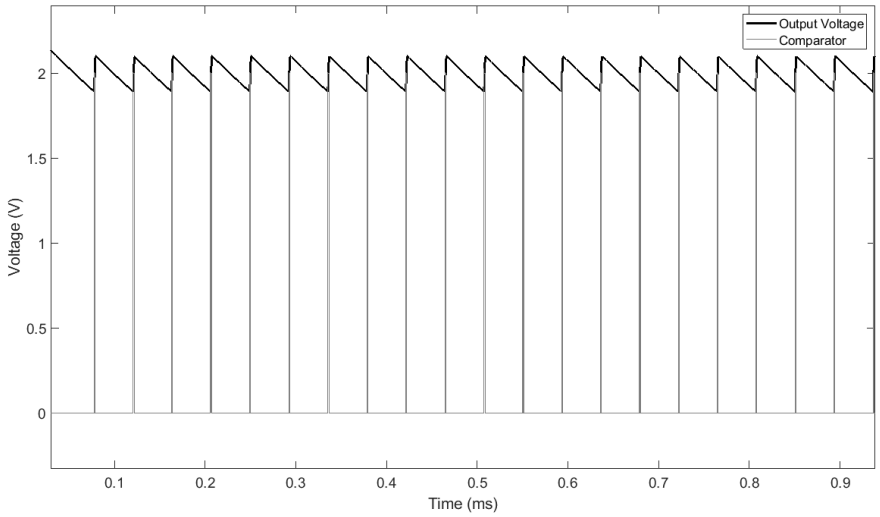

Figure 5.20: Simulation of the buck converter with an input voltage of 30 V, output voltage set to 2 V and an output load resistance of 2 kΩ.

When the regulator's input voltage was set to 40 V in the next simulation, the output voltage is plotted in Figure 5.21. The average steady state output voltage measured 2.05 V, and varies from 1.81 V to 2.15 V, that is a percentage ripple of 8.5 %. The overshoot voltage at startup reached 2.31 V.

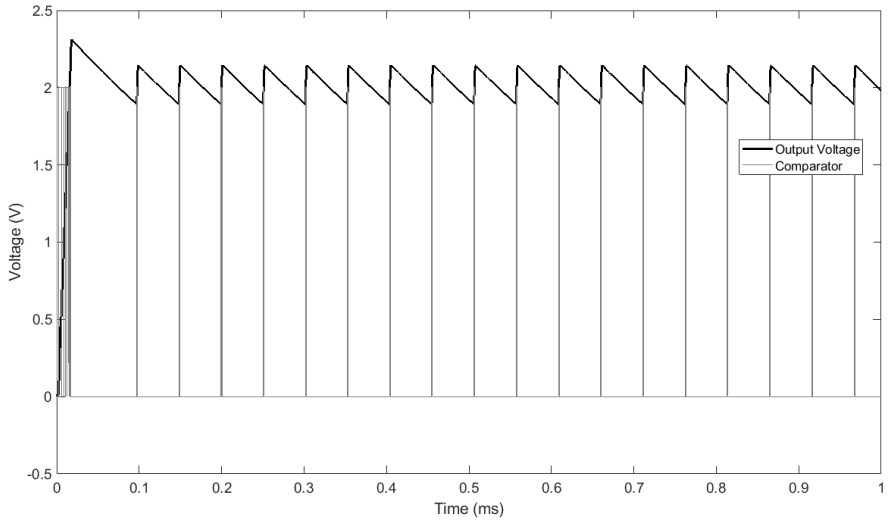

Figure 5.21: Simulation of the buck converter with an input voltage of 40 V, output voltage set to 2 V and an output load resistance of 2 kΩ.

The regulator was then set to generate an output voltage of 5 V. The output load in this simulation is 25 kΩ, which equates to a power of 1 mW, the inductance of the output inductor is 300 µH and the capacitance of the output capacitor is 50 nF. Figure 5.22 plots the comparator output, the gate voltage of the Buck converter high side transistor generated by the bootstrapping circuit and the output voltage. The average output voltage measures 5.0 V, the overshoot voltage reached 5.83 V and then ranged from 4.78 V to 5.10 V, that is percentage ripple voltage of 3.2 %.

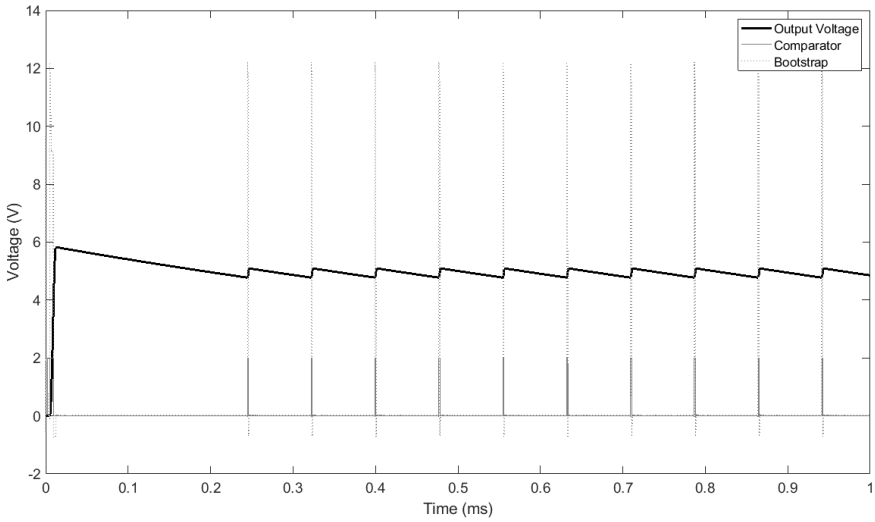

Figure 5.22: Simulation of the buck converter with an input voltage of 10 V, output voltage set to 5 V and an output load resistance of 25 kΩ.

The same simulation with an input voltage of 20 V resulted in a percentage ripple voltage of 10 %. As a mitigation, the output capacitor's capacitance is increased to 100 nF. This simulation is shown in Figure 5.23. It resulted in an average output voltage of 5.03 V, a voltage overshoot of 5.56 V during startup and the output voltage fluctuated from 4.78 V to 5.28 V resulting in a percentage output ripple voltage of 5 %.

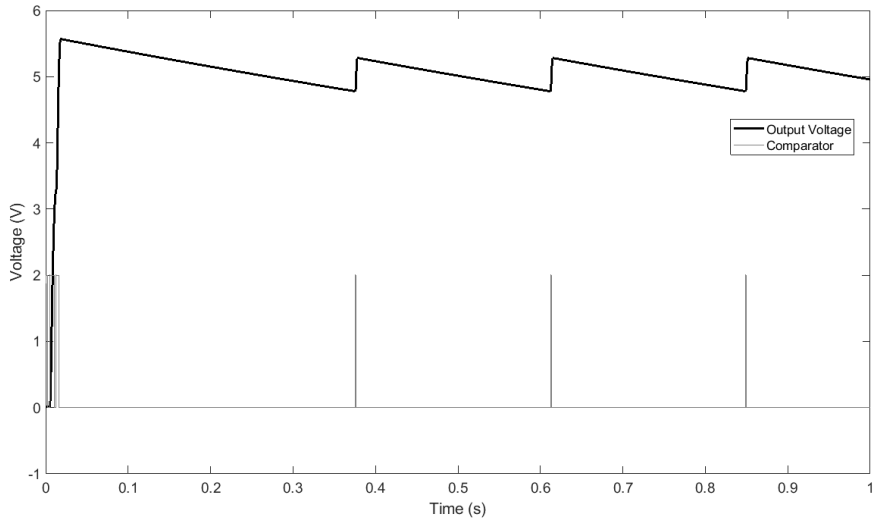

Figure 5.23: Simulation of the buck converter with an input voltage of 20 V, output voltage set to 5 V and an output load resistance of 25 kΩ.

Increasing further the input voltage to 30 V while maintaining the same parameters in the simulation generates the output voltage as shown in Figure 5.24. At this input voltage, the overshoot voltage reaches 5.98 V. It is possible to lower the overshoot voltage, either by increasing the output capacitor's capacitance or by decreasing the inductance of the external inductor of the buck converter. While the former results in a lower output ripple voltage, the latter results in higher ripple voltage on the output. The average output voltage is 5.25 V and the percentage ripple voltage is 10.8 %. Since both overshoot voltage and output ripple voltages are substantial, as a mitigation, the output capacitance should be increased further if the regulator is intended to work at these input conditions. No further changes to the component sizes were carried out in the simulations as the scope of the post-layout simulation was to confirm correct operation of the circuit's internal part. Improving the overshoot and ripple voltages can be obtained externally through the selection of the externally connected output capacitor, output inductor and feedback capacitor. Since the control works by means of a hysteresis control, it is impossible to fully eliminate the output ripple voltage. However, this can be

further reduced by designing and implementing an additional external output R-C or L-C filter.

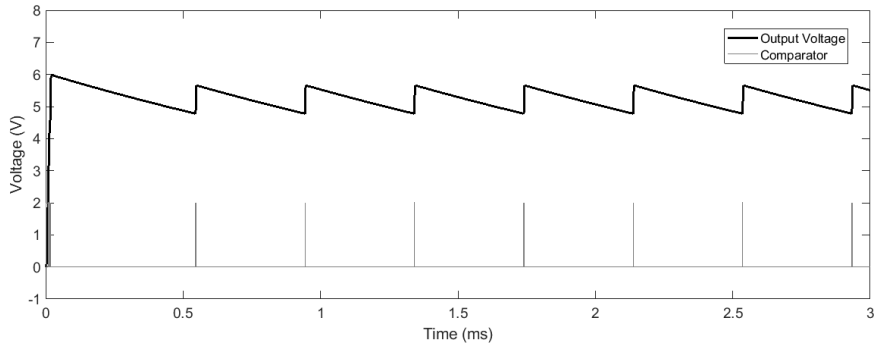

Figure 5.24: Simulation of the buck converter with an input voltage of 30 V, output voltage set to 5 V and an output load resistance of 25 kΩ.

The final post-layout simulation tested the circuit with an input voltage of 40 V. This simulation is shown in Figure 5.25. No overshoot at startup is experienced in this test. The output voltage ranged from 4.78 V to 5.40 V with the average voltage maintained at 5.05 V.

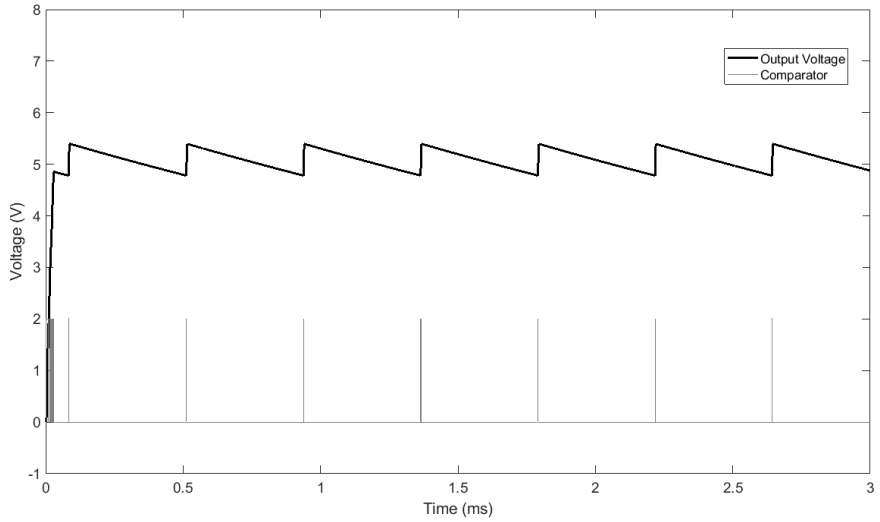

Figure 5.25: Simulation of the buck converter with an input voltage of 40 V, output voltage set to 5 V and an output load resistance of 25 kΩ.

Further post-layout simulations at various temperature, and process conditions were carried out to confirm that these do not affect the circuit operation.

Post-layout simulations showed that the complete circuit works successfully as per set specifications. The peak conversion efficiency of the regulator reaches 82% and the control circuitry consumes an average power of around 500 nW, which is considered negligible for microwatt and milliwatt range energy harvesters.

5.5 Experimental Results

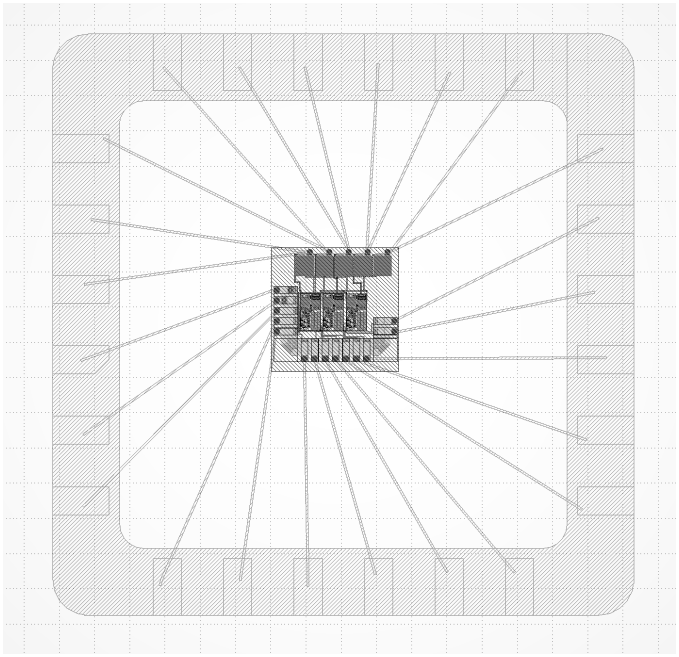

Figure 5.26: Bonding diagram of the integrated circuit to a DIL24 package

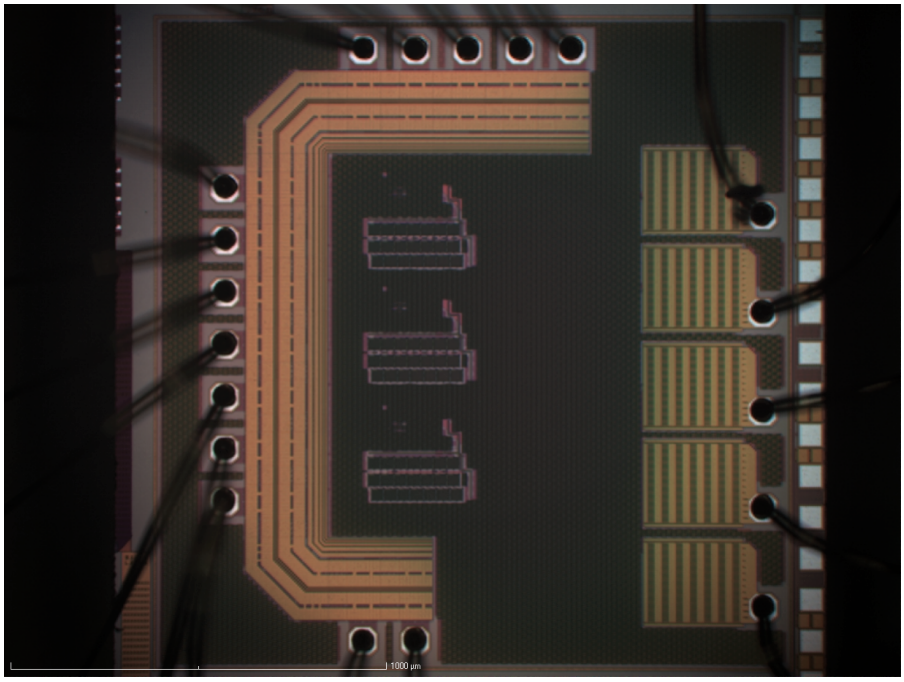

Figure 5.27: Micro photograph of fabricated integrated circuit

Post-layout simulations were carried out to assess the effect of the pads on the total power consumption and the functionality of the circuit blocks. The circuit was sent for fabrication and it was packaged in a DIL24 package. The bonding diagram is shown in Figure 5.26. High voltage, high current pads were bonded to two pins so that a lower impedance is achieved. A micro photograph of the integrated circuit is shown in Figure 5.27.

The fabricated and packaged circuit, was tested and results were extracted for various operation conditions. Figure 5.28 shows a plot of the efficiency versus the conversion ratio at several output voltage conditions when the buck converter is operated at an output current of 2 mA. The efficiency varies from 29% to 84.2%.

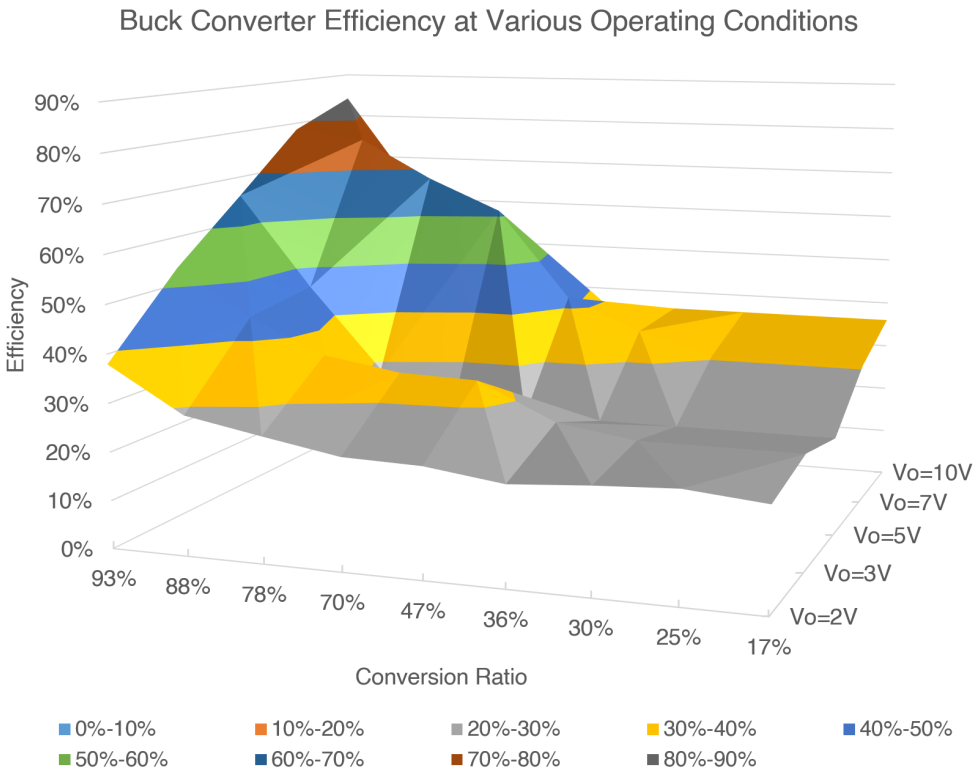

Figure 5.28: Efficiency measurements of the buck converter when operated under different input and output conditions.

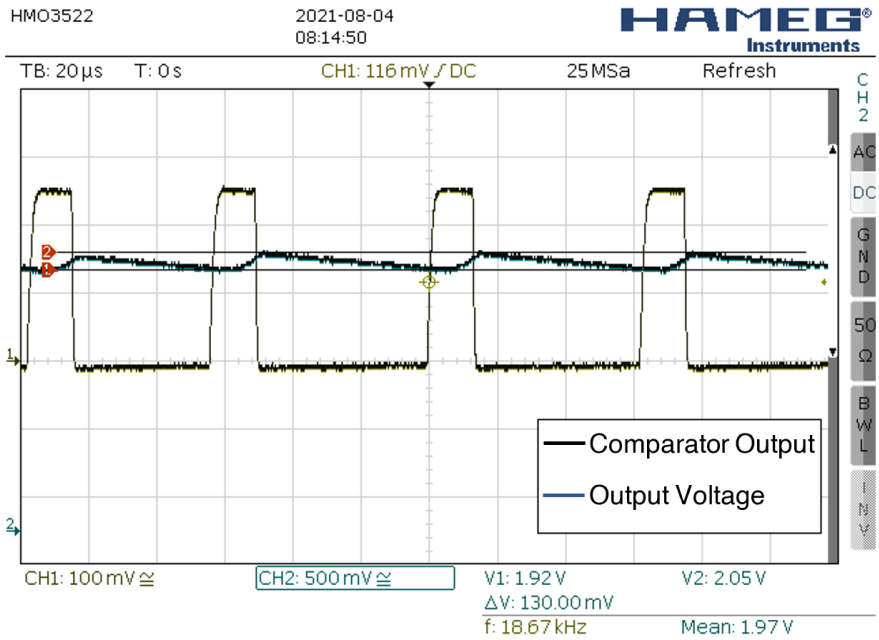

Figure 5.29: Measured comparator output and buck converter output voltage of 2 V from an input voltage of 5 V and an output power of 2 mW.

Figure 5.29 shows the output of the hysteretic control and the output voltage of the buck converter when set to maintain an output of 2 V from an input voltage of 20 V and output power of 2 mW. The percentage ripple output voltage is 6.6% at a frequency of 19 kHz. The ripple voltage and frequency vary depending on the input and output voltage, load current and the hysteretic control biasing current.

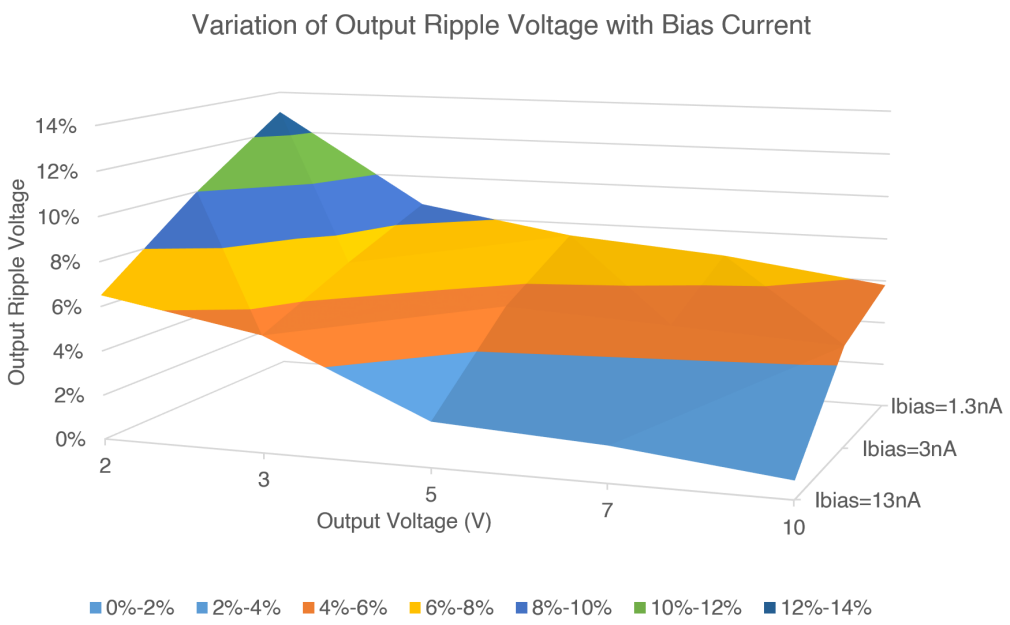

Figure 5.30: Variation of the output ripple Voltage variation with the biasing current of the hysteretic controller.

The circuit was designed in a way to be able to externally control the bias current of the comparator. Therefore, a compromise between the power consumption of the control circuits, the output ripple and response time can be varied externally depending on the requirements. Figure 5.30 shows the percentage output ripple voltage at different bias currents. By lowering the bias current from 13 nA to 1.3 nA, the control circuitry power consumption drops from 420 µW to 194 µW. Post layout simulations showed that the circuit consumes 75 µW at a bias current of 1.3 nA. Additional parasitic capacitances in the interfacing board and low simulator precision in transistors operating in the subtreshold region contribute to the increase in consumption of the control circuit from simulations to practical tests. Nonetheless, the control power consumption is still negligible when compared to the handling power of the converter.

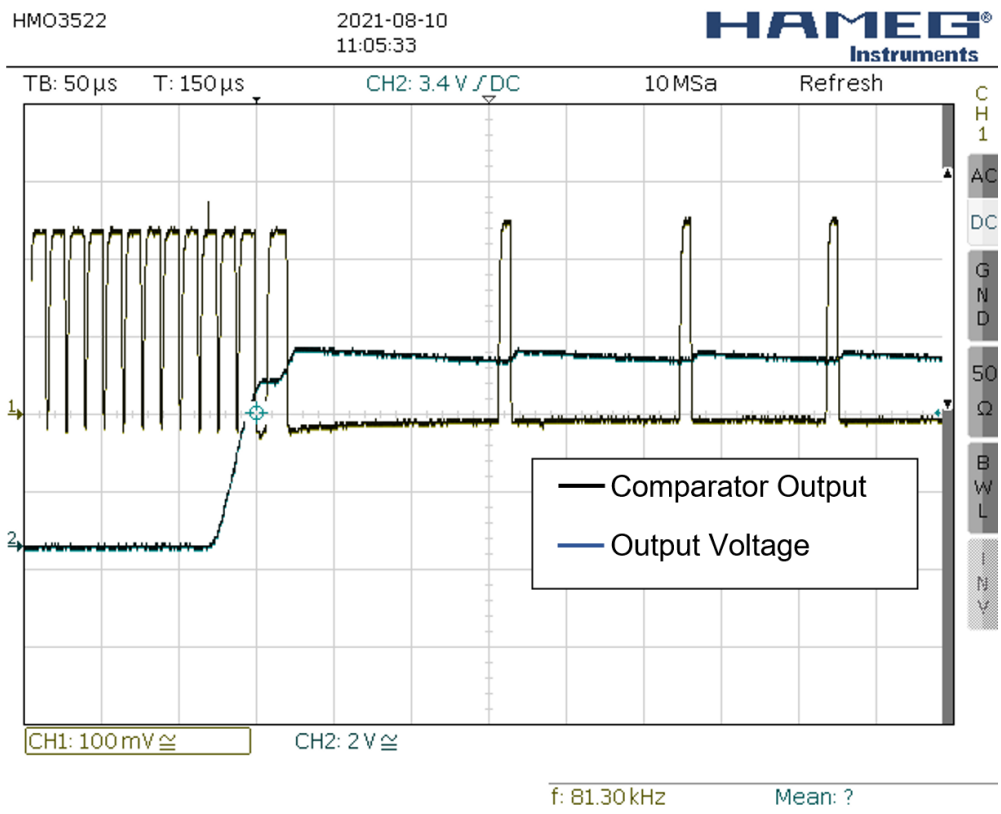

Figure 5.31: Output of the hysteretic comparator and output voltage of the buck converter during startup at an input voltage of 10V and output voltage of 5V.

Hysteretic control tends to have a fast transient response [83]. Figure 5.31 shows the behaviour of the control during startup of the buck converter while stepping down a 10 V input voltage to a 5 V output voltage. The rise time of the buck converter is 49.3 µs. No voltage overshoot was experienced during this test. The same tests were carried out at other output voltages. The rise time for an output voltage of 1 V and 2 V are 14.9 µs and 23.1 µs respectively. No overshoot voltages were experienced in any of the tests.

This circuit was designed in such a way that one of the three buck converters can be able to generate the voltage supply to the control circuits of all three converters. The control circuits require a supply voltage of 2 V. So, one of the buck converters

is adjusted so that its output is 2 V. In order to cold start this converter, a 100 nF capacitor was connected from V_{IN} to the output of the buck converter generating 2 V. This output was also connected to V_{DD} to supply the voltage required to control circuits of all three buck converters. As soon as a voltage is applied to V_{IN}, a voltage is temporarily applied to V_{DD}, which starts up the control circuitry of all the three buck converters. At this point, the buck converter generating this voltage will remain maintaining this voltage indefinitely.

Cold starting this circuit was tested with various input voltages. Figure 5.32 and Figure 5.33 plot the startup of all three buck converters with an input voltage of 8 V and 15 V respectively. It can be noted that the buck converter generating an output voltage of 2 V and is powering the control circuits of all the three buck converters, starts regulating the output from an input voltage of 6 V and so the control circuits do not suffer any overvoltage when the input voltage keeps increasing.

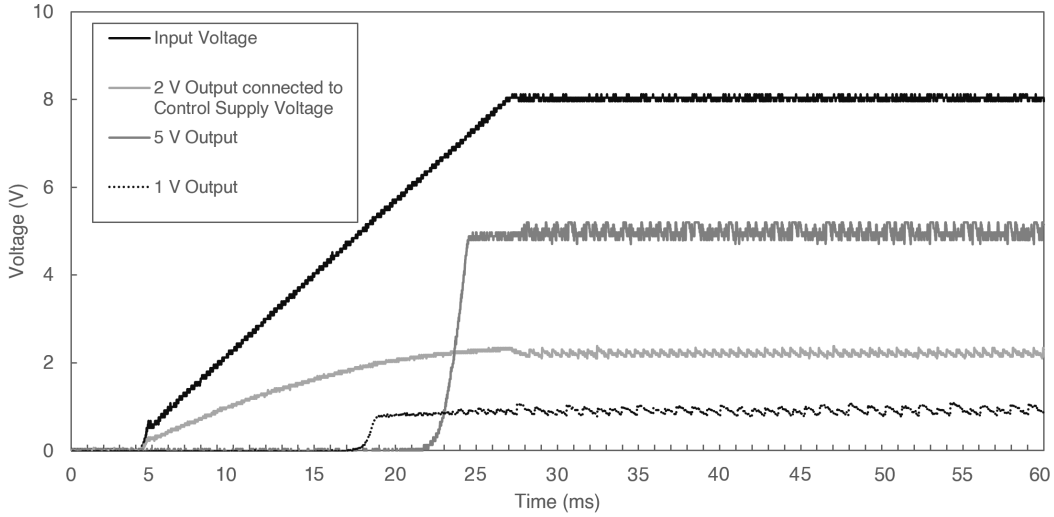

Figure 5.32: Cold starting the three buck converters with an input voltage of 8 V. The control circuits are being powered from the buck converter generating an output voltage of 2 V.

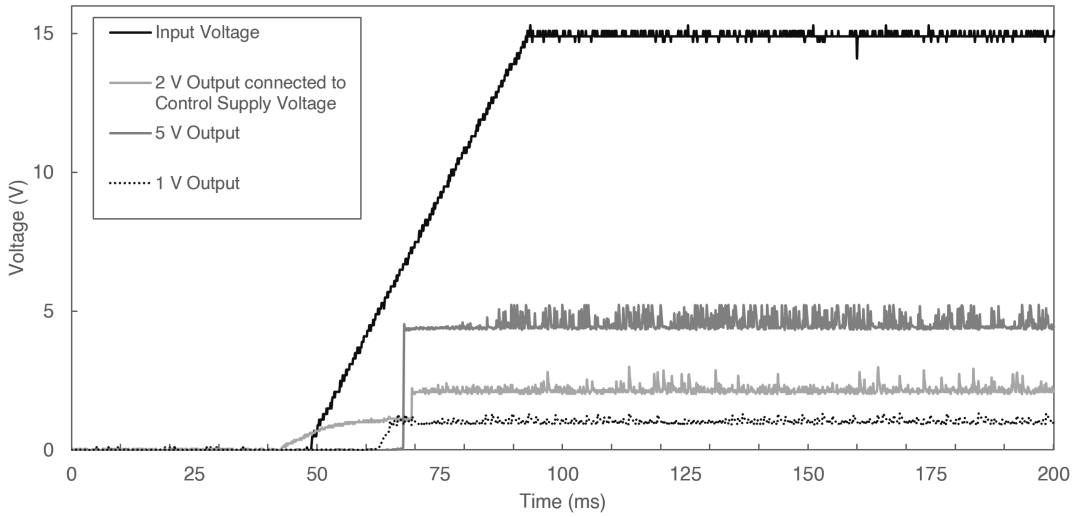

Figure 5.33: Cold starting the three buck converters with an input voltage of 15 V. The control circuits are being powered from the buck converter generating an output voltage of 2 V.

5.6 Conclusion

This chapter presented the design and measured results of the complete testing and characterisation of the buck converter with integrated bootstrap circuit and hysteretic control. These results show that the novel circuitry implemented in this power conditioning circuit, works as predicted by the simulations [14]. The control circuitry consumes between 194 µW to 420 µW, depending on the biasing current at which it is operated. The integrated AC/DC-to-DC converter works as expected with a peak efficiency of 84.2%. The hysteretic control can always maintain the set output voltage and at all input voltages. A compromise between the output ripple voltage and the control circuit power dissipation is possible by varying the bias current of the comparator. Table 5.1 compares the performance of the proposed circuit with that of other state of the art designs reported in literature. This circuit has the widest input and output voltage and power range. It uses the least amount of chip area. Nonetheless, the efficiency levels are very similar to that of the other works, while using either a similar or even cheaper fabrication technology.

	V_{IN}	V_O	η	Area	P_O	Technology
[112]	3.6-36V	5V	86%	$4.78mm^2$	W-range	0.35 µm 60V BCD
[113]	25V	5V	88%	$7mm^2$	W-range	0.2 µm 40V CMOS
[114]	1.8-3.6V	1.2-5.4V	85%	$1.5mm^2$	60mW	180 nm CMOS
[115]	2V	0.4-1.2V	79.8%	$0.38mm^2$	330mW	32nm SOI
This Work	1.5-45V	0.6-40V	84.2%	$0.15mm^2$	100 µW -500mW	0.35 µm 45V X-FAB

Table 5.1: Comparison of the designed buck converter with the SOA.

6. Conclusion and Further Work

This dissertation presented the research carried out on the design and implementation of an energy harvester power conditioning circuit consisting of an AC/DC-to-DC converter with MPPT function and a voltage regulating DC-DC converter. Post layout simulations showed that the ultra-low frequency on-chip oscillators can generate the required frequencies of 15 Hz and 200 kHz reliably over various temperature and fabrication conditions with low power dissipation. In fact, their power consumption is in the nano-watt range while being driven with a supply voltage of 1 V. Simulation results and characterisation carried out on the fabricated prototypes show promising results in the operation of the AC/DC-to-DC Improved Dual Boost converter. The improvements carried out to lower the voltage drops across the parasitic diodes of the switching devices in the converter, from 0.7 V to 0.45 V ensured better conversion efficiency. These improvements achieve a better efficiency in all four modes of operation of the converter. Designing circuits in the subthreshold region with currents in the nano-ampere range is challenging especially due to temperature and fabrication variations. When designing, simulating, and testing the circuits at block level, all circuits were simulated within the following temperature range 0 °C and 80 °C together with fabrication corner conditions mainly at worst speed and at worst power. While changes were noticed in all the circuit stages, before finalising the design, it was ensured that these changes do not adversely affect the correct

operation of the circuit. Finally, a design with all its internal circuits capable to work within this temperature range and at corner conditions was obtained. In the layout stage, special attention was given to the shielding of the converter and the gate drive from the rest of the control circuits. The final design of the converter with MPPT power conditioning circuit without pads measures 347 µm by 289 µm. This means that this power conditioning circuit occupies just $0.1mm^2$. The circuit has a total of twenty pads. However, most of these pads are only required for prototyping and testing purposes. The circuit's dimensions including pads is 1.3 mm by 1.3 mm. This means that the power conditioning circuit occupies $1.7mm^2$. The essential pads of the final charge conditioning circuit consist of only four pads which are the connections to the energy harvester and the output voltage. Since the supply voltages to this part of the circuit will be generated by the Voltage Regulating DC-DC converter, which was designed and fabricated at a later stage, these voltage supplies are supplied externally. Hence for this circuit since this is just the first stage of the circuit two additional pads for supply are required. This circuit should be capable to cold start once the energy harvester generates a voltage of 1 V. Since the rectification is done in the Boost converter itself, this increases the overall efficiency of the power conditioner. This circuit is capable to work with various energy harvesting types and models due to the MPPT algorithm adopted which is capable to sense the maximum power point of different types of energy harvesting devices mainly because the power-voltage curve is similar amongst all energy harvesters. The MPPT controller is designed to depend on only one input feedback signal which is the output voltage of the Dual Boost converter. Having one feedback signal saves energy since it does not require multipliers as in other power conditioning architectures reported in literature. Consequently, this research confirmed that a voltage feedback is more efficient than a current feedback, since the latter consumes power due to the employment of a shunt resistor.

The second fabricated circuit is the hysteretic controlled Buck converter with

capacitively coupled bootstrapping circuit which complements the first part of the circuit to obtain a complete power conditioning circuit. This integrated circuit consists of three similar buck converters which are designed to generate the 1 V supply voltage for the control circuits of the first circuit, the 2 V supply voltage for the control circuits of the first and second circuit and another voltage supply as required by the load. The output voltage of the three converters can be set externally by means of a feedback resistor. The control of these converters is by an analogue hysteretic control which is designed for minimum power consumption. A compromise between output ripple voltage and bias current can be found depending on the required output. An externally connected capacitor can also be connected to lower the overshoot in the output voltage during startup, since it would emulate a derivative component in the feedback loop. The converter also requires an externally connected inductor and output capacitor, and their values can be adjusted depending on the conditions at which the converter will be operating.

The control circuitry works with a supply voltage of 2 V and the Buck converter has a maximum operating voltage of 45 V. The ideal switching transistor to be used in a Buck converter is a PMOS high voltage transistor. This would guarantee a simple yet effective design. The gate oxide of the transistor had to be thin so that it could be switched on with a gate voltage of just 2 V. However, the X-FAB H35 fabrication technology does not have a high voltage PMOS transistor having a thin gate oxide layer. The only high voltage transistor with a thin gate oxide layer is an NMOS transistor. This problem is also present in most of today's high voltage fabrication technology. For this reason, the only way to drive the Buck converter was by including a bootstrapping circuit so that the gate voltage applied to the high voltage NMOS transistor is raised high enough for it to operate in the ohmic region. An on-chip innovative bootstrapping circuit capacitively coupled with a low voltage hysteretic control was thus proposed and implemented. The control

circuitry consumes between 194 µW to 420 µW, depending on the biasing current at which it is operated. The integrated Buck converter worked as expected with a peak power conversion efficiency of 84.2%. The hysteretic control can always maintain the set output voltage and at all input voltages. This circuit has the widest input and output voltage and power range and uses the least amount of chip area when compared to the state of art. Nonetheless, the efficiency levels are very similar to that of the other works, while using either a similar or even cheaper fabrication technology.

The final designed power conditioning circuit is capable to work with various energy harvesters within the input voltage and power range compatible with the designed circuit. This conditioning circuit can maintain MPPT and has energy storage capability in a high storage capacitor. The circuit includes a buck converter with adjustable regulated output voltage, which can be set according to the load being connected.

This power conditioning circuit which consists of the two integrated circuits, has most of the functions required to be able to work with various energy harvesters and various loads. That is why its design includes MPPT, capacitive energy storage, AC and DC input voltages, and regulated output voltage. However, some applications may require only one of the two stages. In this case, eliminating one of the stages would lead to a higher energy efficiency. If an application should require only one stage, the contribution to knowledge in its respective design and operation, can still be applied without the other stage. For example, in case a power conditioning circuit will not be connected to an energy harvester generating an AC voltage, the same control circuit can be used to drive a normal Boost converter instead of the Improved Dual Boost converter. This leads to a higher conversion efficiency due to less switching components. If the power conditioning circuit will be connected to an energy harvester producing high voltage, then the buck converter stage is enough and the MPPT should be implemented to the buck converter.

Sections of the work discussed in this dissertation were published in a number of peer reviewed publications indicating the validity of the research. In addition, this work can be extended to other research paths which could be followed in the future. The following is a list of some of the possible research avenues:

- Both switching devices in the improved dual boost converter are switched on simultaneously. However, when working with a DC input voltage only one of the switching devices is conducting current while the other is being switched for no reason. This approach eliminated the need of a polarity sensing circuit while still capable to work with AC input voltages. However, it may be the case that the losses incurred in gate charging the extra switching device is higher than a polarity sensing block. Furthermore, if the converter is being designed to work only with energy harvesters generating a DC voltage, a normal boost converter will have less switching devices than the improved dual boost converter and hence, a better conversion efficiency can be obtained.

- The improved dual boost converter can have a number of switching devices with different sizes so that these are switched on depending on the current handling power of the converter. This approach maximises the power efficiency through a wider power window by switching on only the required amount of switching devices. This gives the opportunity to get a compromise between the gate charging losses and the conduction losses.

- The proposed power conditioning circuit consisting of two integrated circuits, has most of the functions required to be able to work with various energy harvesters and various loads. That is why its design includes MPPT, capacitive energy storage, AC and DC input voltages, and regulates the output voltage. However, these two stages can be implemented as independent circuits leading to a higher energy efficiency. If an application should require only one stage, the contribution to knowledge in its respective

design and operation, can still be applied without the other stage. For example, in case a power conditioning circuit will not be connected to an energy harvester generating an AC voltage, the same control circuit can be used to drive a normal Boost converter instead of the Improved Dual Boost converter. This leads to a higher conversion efficiency due to less switching components. If the power conditioning circuit will be connected to an energy harvester producing high voltage, then the buck converter stage is enough and the MPPT should be implemented to the buck converter.

- The overall area of the proposed circuit is relatively small. Depending on the final application, it might be worthwhile consuming some additional area in order to obtain a better conversion efficiency. Possible improvements to obtain a better conversion efficiency in the converters fabricated are: increase the sizes of the high voltage transistors in the switch mode converter, paralleling of pads and track widening of connections carrying the input and output currents of the converter are all possible improvements which lowers the conduction losses and as a result increase the conversion efficiency.

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A. Analysis of Current Reference Circuit

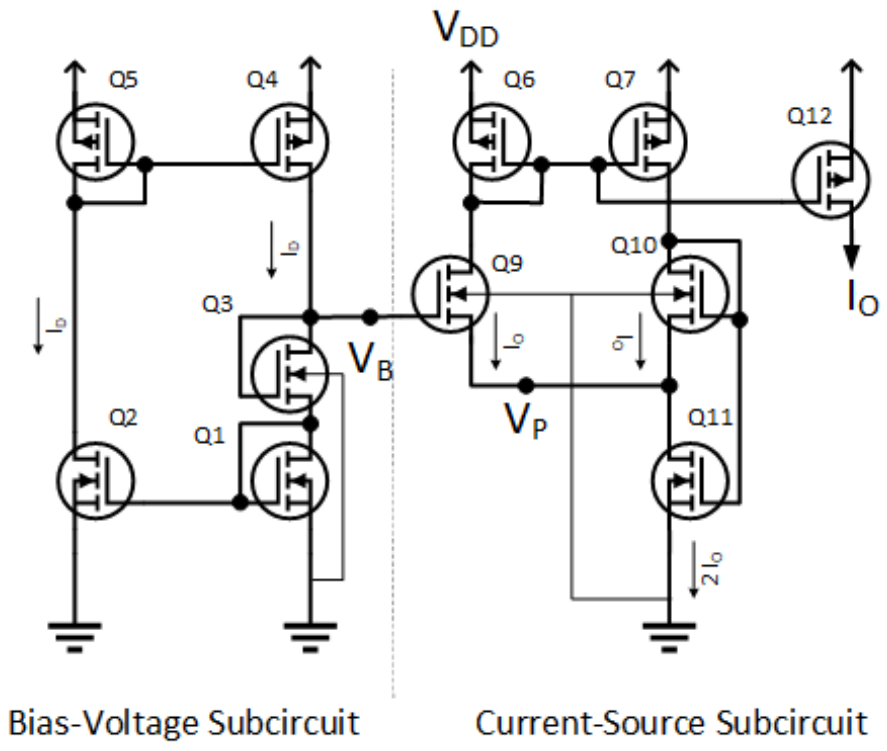

Figure A.1: Self-biased temperature and supply voltage independent current reference circuit using CMOS MOSFETs operating in the subthreshold region modified for lower power consumption

$$V_B = V_{GS1} + V_{GS3} \tag{A.1}$$

$$I_{D1} = I_{D_O1} K_1 e^{\frac{V_{GS1} - V_{T1}}{nV_t}} \tag{A.2}$$

$$V_{GS1} = nV_t \ln\left(\frac{I_{D1}}{I_{D_O1} K_1}\right) + V_{T_1} \tag{A.3}$$

$$I_{D3} = I_{D_O3} K_1 e^{\frac{V_{GS3} - V_{T3}}{nV_t}} \tag{A.4}$$

$$V_{GS3} = nV_t \ln\left(\frac{I_{D3}}{I_{D_O3} K_3}\right) + V_{T_3} \tag{A.5}$$

$$I_D = I_{D_1} = I_{D_2} = I_{D_3} \tag{A.6}$$

where V_{GS} is the gate to source voltage, I_D is the drain current, V_T is the threshold voltage, I_{Do} is the drain current when V_{GS}=V_T, K_n is the aspect ratio of the transistor n, V_t is the thermal voltage and n is the slope factor.

Substituting Eq. A.3, Eq. A.5 and Eq. A.6 into Eq. A.1;

$$V_B = V_{T_1} + V_{T_3} + nV_t \ln\left(\frac{I_D}{I_{D_O1} K_1}\right) + nV_t \ln\left(\frac{I_D}{I_{D_O3} K_3}\right) \tag{A.7}$$

$$V_B = V_{T_1} + V_{T_3} + nV_t \left[\ln\left(\frac{I_D}{I_{D_O1} K_1}\right) + \ln\left(\frac{I_D}{I_{D_O3} K_3}\right)\right] \tag{A.8}$$

$$I_D = I_{D2} = I_{D_O2} K_2 e^{\frac{V_{GS2} - V_{T2}}{nV_t}} \tag{A.9}$$

$$V_{GS2} = V_B - V_{GS3} \tag{A.10}$$

$$I_D = I_{D_O2} K_2 e^{\frac{V_B - V_{GS3} - V_{T2}}{nV_t}} \tag{A.11}$$

Replacing I_D in Eq. A.8 by Eq. A.11;

$$V_B = V_{T_1} + V_{T_3} + nV_t \left[\ln \left(\frac{I_{D_O}2K_2 e^{\frac{V_B - V_{GS3} - V_{T2}}{nV_t}}}{I_{D_O}1K_1} \right) + \ln \left(\frac{I_{D_O}2K_2 e^{\frac{V_B - V_{GS3} - V_{T2}}{nV_t}}}{I_{D_O}3K_3} \right) \right] \tag{A.12}$$

$$V_B = V_{T_1} + V_{T_3} + nV_t \left[\ln \left(\frac{I_{D_O}2K_2}{I_{D_O}1K_1} \right) + \frac{V_B - V_{GS3} - V_{T2}}{nV_t} + \ln \left(\frac{I_{D_O}2K_2}{I_{D_O}3K_3} \right) + \frac{V_B - V_{GS3} - V_{T2}}{nV_t} \right] \tag{A.13}$$

$$V_B = V_{T_1} + V_{T_3} + nV_t \left[\ln \left(\frac{I_{D_O}2K_2}{I_{D_O}1K_1} \right) + \ln \left(\frac{I_{D_O}2K_2}{I_{D_O}3K_3} \right) + 2 \left(\frac{V_B - V_{GS3} - V_{T2}}{nV_t} \right) \right] \tag{A.14}$$

$$V_B = 2V_B - 2V_{GS3} - 2V_{T2} + V_{T1} + V_{T3} + nV_t \left[\ln \left(\frac{I_{D_O}2K_2}{I_{D_O}1K_1} \right) + \ln \left(\frac{I_{D_O}2K_2}{I_{D_O}3K_3} \right) \right] \tag{A.15}$$

$$-V_B = -2V_{GS3} - 2V_{T2} + V_{T1} + V_{T3} + nV_t \left[\ln \left(\frac{I_{D_O}2K_2}{I_{D_O}1K_1} \right) + \ln \left(\frac{I_{D_O}2K_2}{I_{D_O}3K_3} \right) \right] \tag{A.16}$$

$$I_{D_O}1 = I_{D_O}2 \tag{A.17}$$

$$K_1 = K_2 \tag{A.18}$$

$$V_B = 2V_{GS3} + 2V_{T2} - V_{T1} - V_{T3} - nV_t \left[\ln \left(\frac{I_{D_O}1K_1}{I_{D_O}1K_1} \right) + \ln \left(\frac{I_{D_O}1K_1}{I_{D_O}3K_3} \right) \right] \tag{A.19}$$

$$V_B = 2V_{GS3} + 2V_{T2} - V_{T1} - V_{T3} - nV_t \ln \left(\frac{I_{D_O}1K_1}{I_{D_O}3K_3} \right) \tag{A.20}$$

$$V_{T2} \approx V_{T1} \tag{A.21}$$

$$V_B = -nV_t \ln \left(\frac{I_{D_O}1K_1}{I_{D_O}3K_3} \right) + 2V_{GS3} + V_{T2} - V_{T3} \tag{A.22}$$

$$V_P = V_{GS11} - V_{GS10} \tag{A.23}$$

$$V_{GS10} = nV_t \ln\left(\frac{I_{D10}}{I_{D_O10}K_{10}}\right) + V_{T10} \tag{A.24}$$

$$V_{GS11} = nV_t \ln\left(\frac{I_{D11}}{I_{D_O11}K_{11}}\right) + V_{T11} \tag{A.25}$$

$$I_O = I_{D10} = I_{D9} \tag{A.26}$$

$$I_{D11} = 2I_{D10} = 2I_O \tag{A.27}$$

$$V_{GS11} = nV_t \ln\left(\frac{2I_{D10}}{I_{D_O11}K_{11}}\right) + V_{T11} \tag{A.28}$$

Substituting Eq. A.28 and Eq. A.24 in Eq. A.23;

$$V_P = \ln\left(\frac{2I_{D10}}{I_{D_O11}K_{11}}\right) nV_t + V_{T11} - \ln\left(\frac{I_{D10}}{I_{D_O10}K_{10}}\right) nV_t - V_{T10} \tag{A.29}$$

$$V_P = nV_t\left[\ln\left(\frac{2I_{D10}I_{D_O10}K_{10}}{I_{D10}I_{D_O11}K_{11}}\right)\right] + V_{T11} - V_{T10} \tag{A.30}$$

$$I_{D_O10} = I_{D_O11} \tag{A.31}$$

$$V_P = nV_t\left[\ln\left(\frac{2K_{10}}{K_{11}}\right)\right] + V_{T11} - V_{T10} \tag{A.32}$$

$$I_O = I_{D_0 9}K_9 e^{\frac{V_B - V_P - V_{T9}}{nV_t}} \tag{A.33}$$

Considering $\frac{V_B - V_P - V_{T9}}{nV_t}$

$$\frac{V_B - V_P - V_{T9}}{nV_t} = \frac{-nV_t \ln\left(\frac{I_{D_O1}K_1}{I_{D_O3}K_3}\right) + 2V_{GS3} + V_{T1} - V_{T3} - nV_t \ln\left(\frac{2K_{10}}{K_{11}}\right) - V_{T11} + V_{T10} - V_{T9}}{nV_t} \tag{A.34}$$

$$\frac{V_B - V_P - V_{T9}}{nV_t} = \ln\left(\frac{I_{D_O3}K_3K_{11}}{2I_{D_O1}K_1K_{10}}\right) + \frac{2V_{GS3} + V_{T1} - V_{T3} - V_{T11} + V_{T10} - V_{T9}}{nV_t} \tag{A.35}$$

Let

$$\delta V_{TH} = V_{T_1} + V_{T_{10}} - V_{T_3} - V_{T_9} - V_{T_{11}} \tag{A.36}$$

$$\frac{V_B - V_P - V_{T9}}{nV_t} = \ln\left(\frac{I_{D_O3}K_3K_{11}}{2I_{D_O1}K_1K_{10}}\right) + \frac{2V_{GS3} + \delta V_{TH}}{nV_t} \tag{A.37}$$

$$I_O = I_{D_0}K_9 e^{\ln\left(\frac{I_{D_O3}K_3K_{11}}{2I_{D_O1}K_1K_{10}}\right)} e^{\frac{2V_{GS3}+\delta V_{TH}}{nV_t}} \tag{A.38}$$

$$I_O = I_{D_0}\frac{K_9 I_{D_O3}K_3K_{11}}{2I_{D_O1}K_1K_{10}} e^{\frac{2V_{GS3}+\delta V_{TH}}{nV_t}} \tag{A.39}$$

Eq. A.39 has the form of

$$I_O = Ae^{\frac{B}{nV_t}} \tag{A.40}$$

$$V_t = \frac{kT}{q} \tag{A.41}$$

$$I_O = Ae^{\frac{Bq}{nkT}} \tag{A.42}$$

where k is Boltzmann's constant, T is the absolute temperature and q is the elementary charge.

Solving for the temperature coefficient $\frac{\delta I_O}{\delta T}$ which should be equal to zero.

$$\frac{\delta I_O}{\delta T} = -ABq\frac{e^{\frac{Bq}{nkT}}}{nkT^2} = 0 \tag{A.43}$$

$$0 = -\frac{1}{Ae^{\frac{Bq}{nkT}}}\frac{ABqe^{\frac{Bq}{nkT}}}{nkT^2} \tag{A.44}$$

$$0 = -\frac{Bq}{nkT^2} \tag{A.45}$$

$$0 = -\frac{B}{nV_TT} \tag{A.46}$$

$$0 = -\frac{2V_{GS3} + \delta V_{TH}}{nV_TT} \tag{A.47}$$

$$\delta V_{TH} = -2\ V_{GS3} \tag{A.48}$$

where $\delta V_{TH} = V_{T_1} + V_{T_{10}} - V_{T_3} - V_{T_9} - V_{T_{11}}$ and K is the transistor aspect ratio. In order to obtain a zero temperature coefficient circuit, δV_{TH} should be equal to $-2\ V_{GS3}$.

B. Physical Circuit Layout Design

The integrated circuit physical layout was designed out once all the simulations including corner analysis showed a successful operation of the circuit. The layout had to take into consideration the noise generated by the high power improved dual boost converter and its respective PWM generation comparator from affecting the rest of the circuitry. The rest of the circuitry being the control circuitry, is very prone to noise because of the voltage signals. Due to the low power requirements of this circuit, the low currents involved in the control circuitry are in the nA range. Such a small current decreases the signal to noise ratio. Apart from the matching of transistors in current mirrors, and differential amplifiers, shielding and adequate spacing were the precautions taken to reduce the noise generated in the control MPPT circuitry. Another aspect which had to be considered in the layout design is the high currents and voltages involved in the power circuitry. High currents require sufficiently wide and thick metal interconnects so that no damage is done by the continuous current during normal operation and to reduce the voltage drop across these metal interconnects. Furthermore, the metal interconnects are sufficiently spaced to take into account the high electric field requirement due to the high voltage requirements. Another problem which was addressed is that since the inductor and output capacitor are externally connected, the combined inductance and resistance of the pads and metal interconnects between the inductor and the switching devices and between the diode connected transistors and the output

capacitor would create voltage overshoots during the switching off of the switching devices.

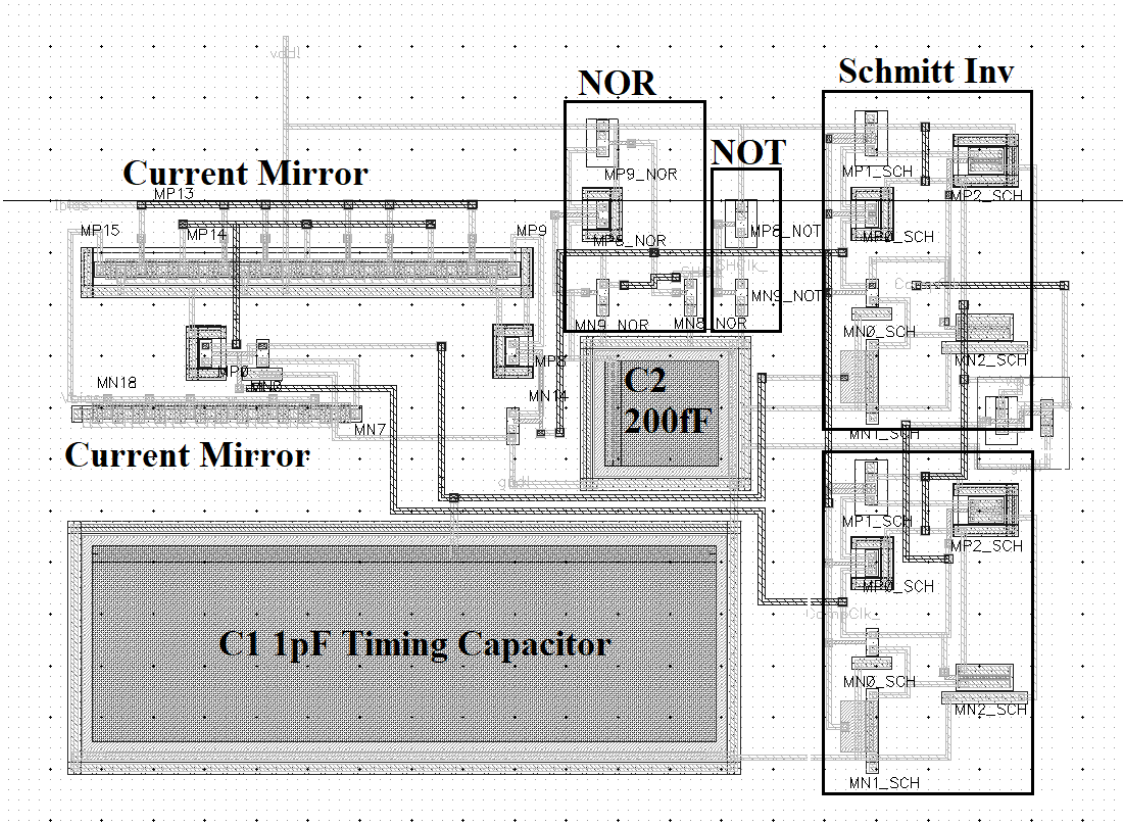

Figure B.1: Layout implementation of the 15 Hz oscillator as fabricated into the integrated circuit

The layout of the 15 Hz oscillator is shown in Figure B.1. The main parts of the circuit are labelled. The two timing capacitors; *C1* and *C2*, are the timing capacitor for the 15 Hz oscillator and the timing capacitor for the Sample and Hold clock pulse respectively. The two Schmitt inverters which are part of the positive feedback loop and the NOR and OR gates essential to generate the Sample and Hold clock pulse are also shown. The transistors of the two current mirrors are matched using the interdigitated matching technique. A guard ring is constructed around both capacitors. All PMOS transistors include an n-well tie and all NMOS transistors include a substrate tie to as many sides as possible. These ties guarantee the best

possible connection between the source and body of the transistors and also serve for noise shielding.

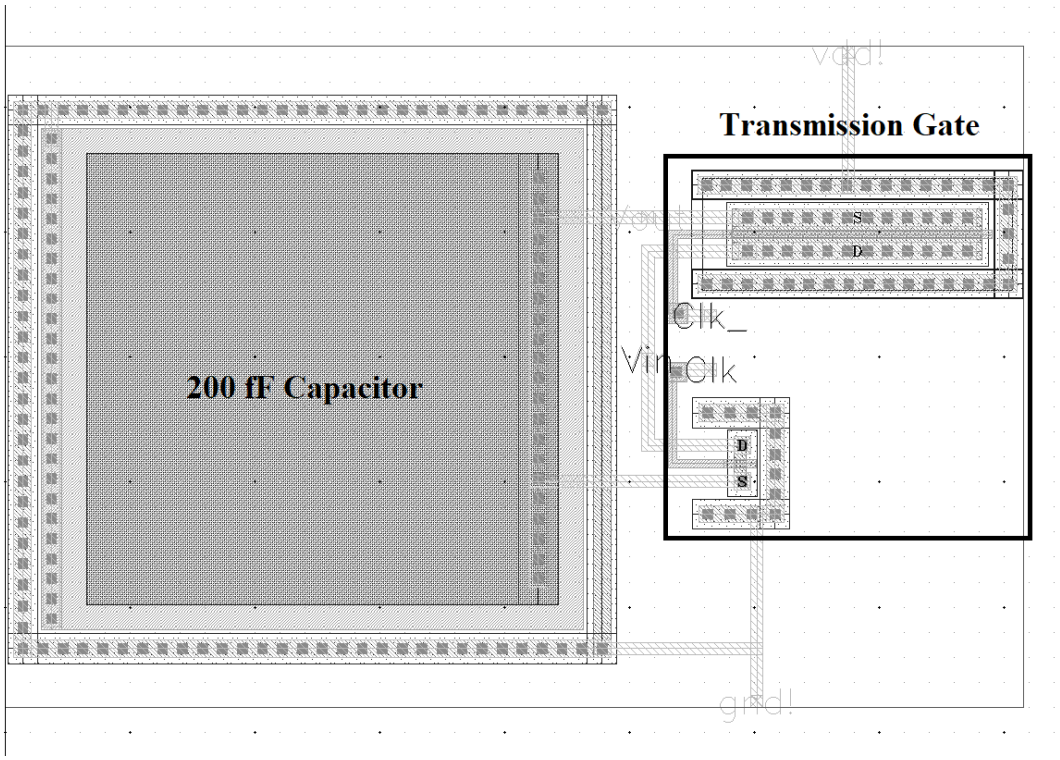

Figure B.2: Layout implementation of the Sample and Hold circuit as fabricated into the integrated circuit

The Sample and Hold circuit consists of a 200 fF capacitor and a transmission gate. The circuit layout is shown in Figure B.2. A guard ring is implemented around the sides of the capacitor. On the right hand side, the guard ring is continued without the Metal 1 so that connections can be routed inside, towards the plates of the capacitor.

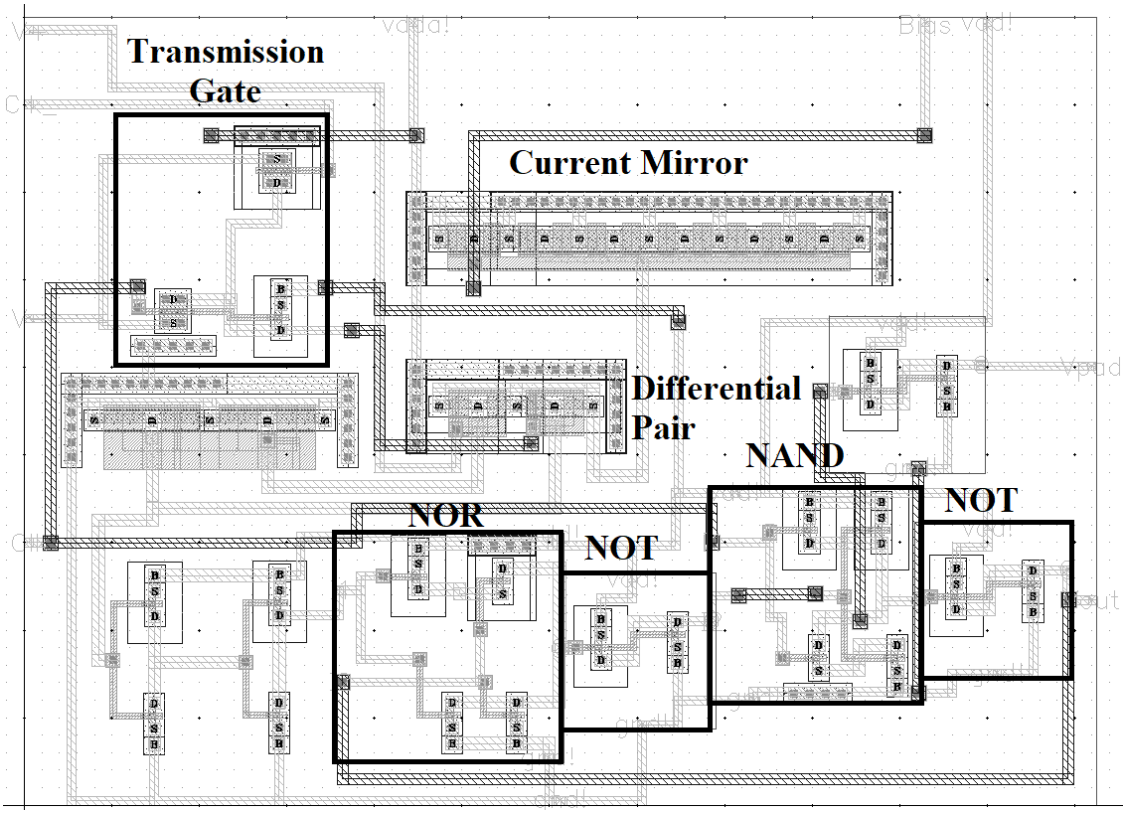

Figure B.3: Layout implementation of the clocked comparator as fabricated into the integrated circuit

The circuit layout of the clocked comparator is shown in Figure B.3. The gates required to latch the output, the differential pair, transmission gate as part of the clock and the current mirror are all labelled in the figure. The current mirror and the differential pair of the comparator and the current mirror generating the bias current to the comparator use interdigitated matched transistors technique. Substrate ties around the matched transistors are used to get the best possible connection between the source and the body of the transistors.

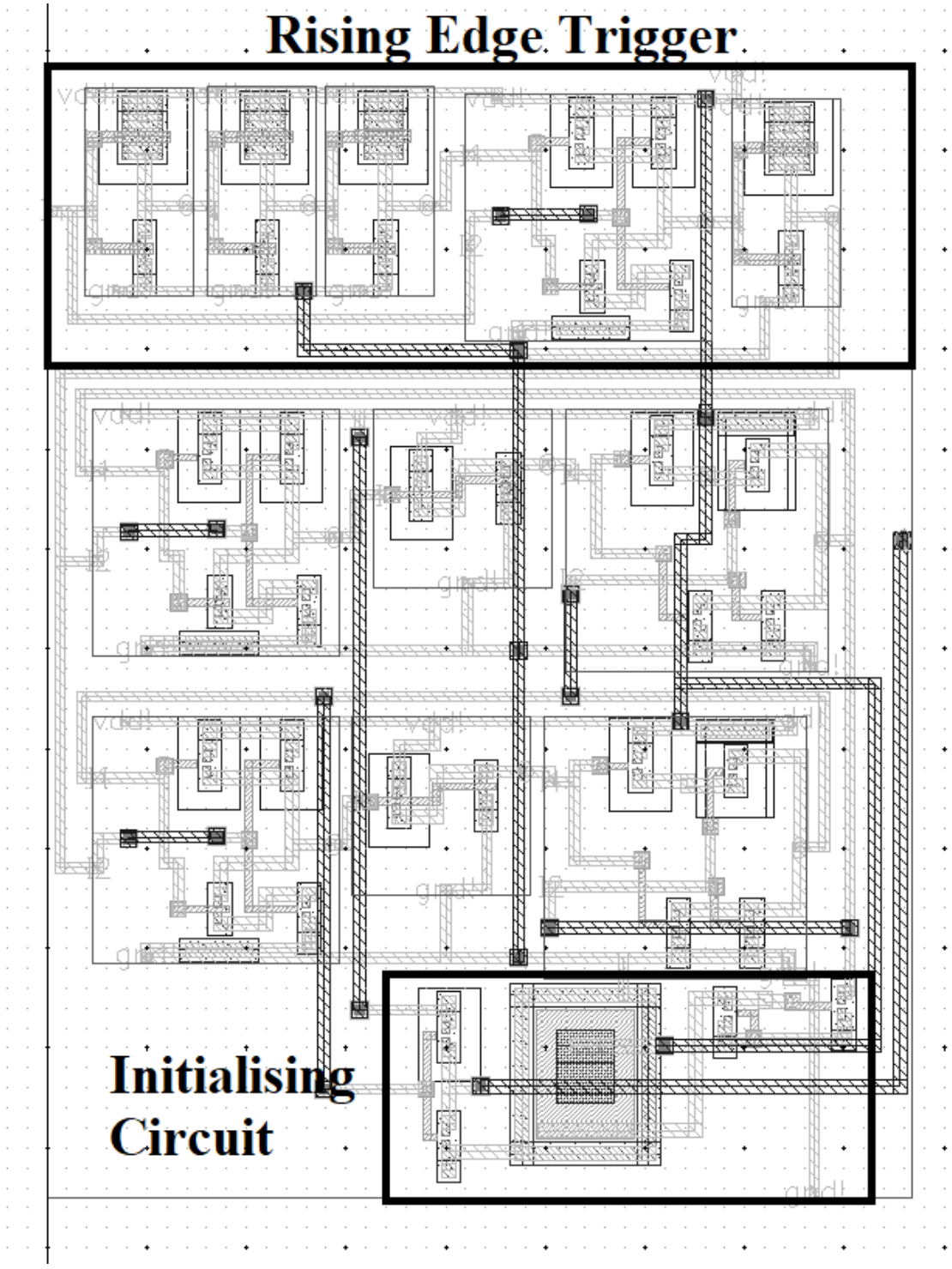

Figure B.4: Layout implementation of the Toggle Flip-Flop as fabricated into the integrated circuit

The circuit layout of the Toggle Flip-Flop shown in Figure B.4, consists of a rising edge trigger, the flip-flop itself and the initialising circuit to ensure that the flip-flop's output Q initialises at a low state.

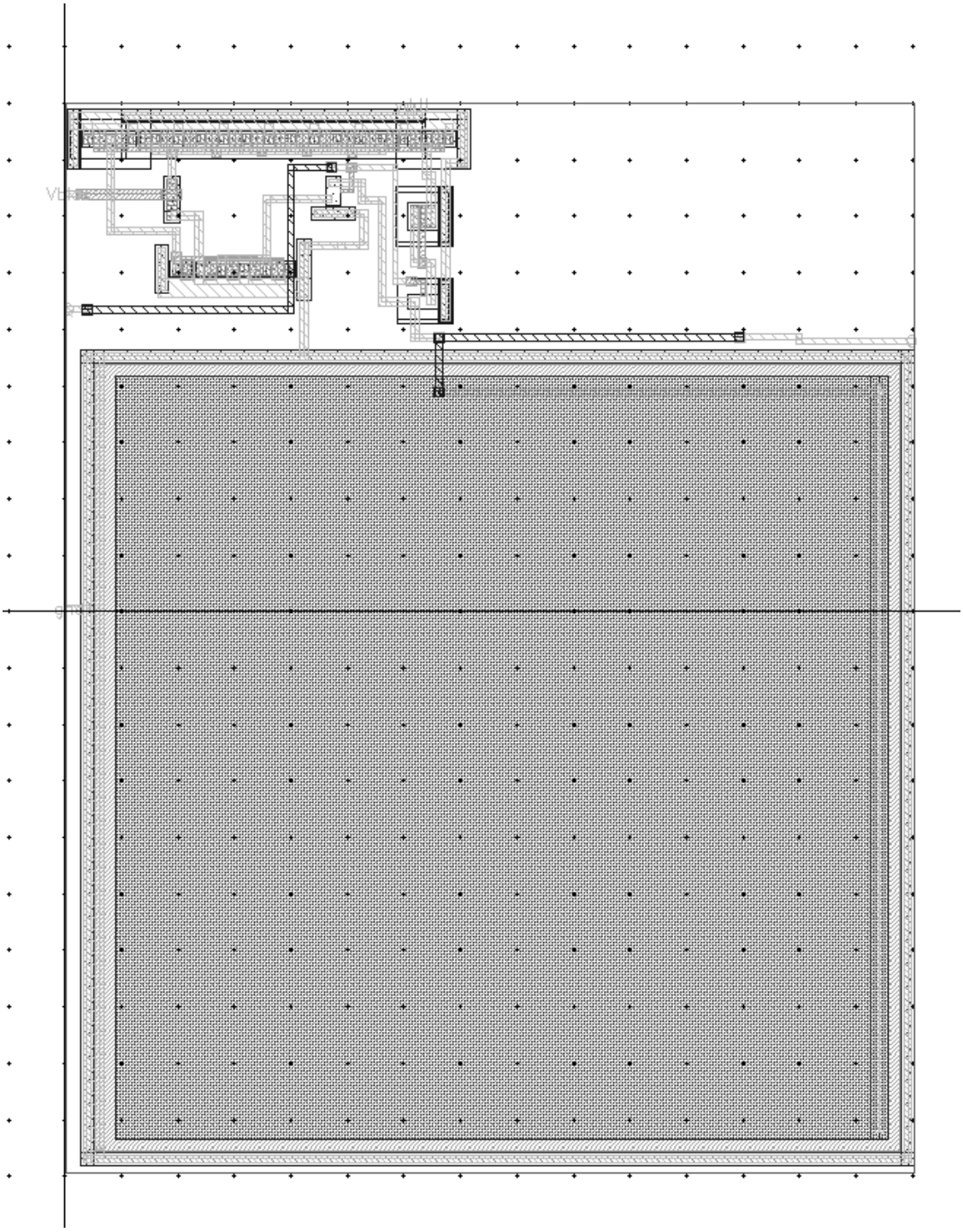

Figure B.5: Layout implementation of the charge pump as fabricated into the integrated circuit

The charge pump layout shown in Figure B.5, consists of two current mirrors to

current starve the charging and discharging currents of the capacitor and a 2 pF capacitor. Both current mirrors use the interdigitated matching technique. This circuit is most susceptible to noise due to the low charging and discharging currents of the capacitor.The capacitor is protected from noise by a guard ring and the transistors use substrate ties on most of their sides.

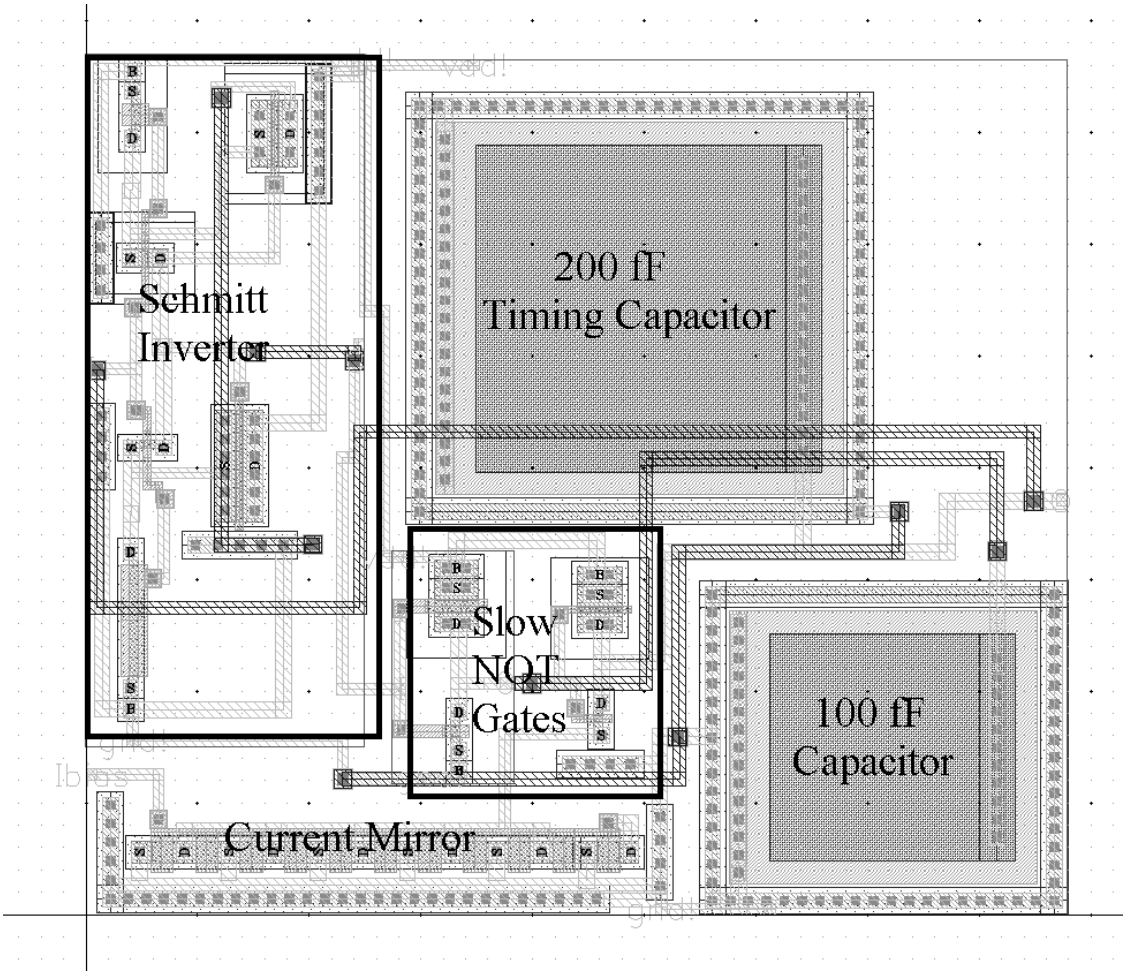

Figure B.6: Layout implementation of the 200 kHz sawtooth generator as fabricated into the integrated circuit

The layout of the 200 kHz sawtooth generator is shown in Figure B.6. A current mirror for the current starved inverter, the timing capacitors and the Schmitt inverter are labelled in the diagram.

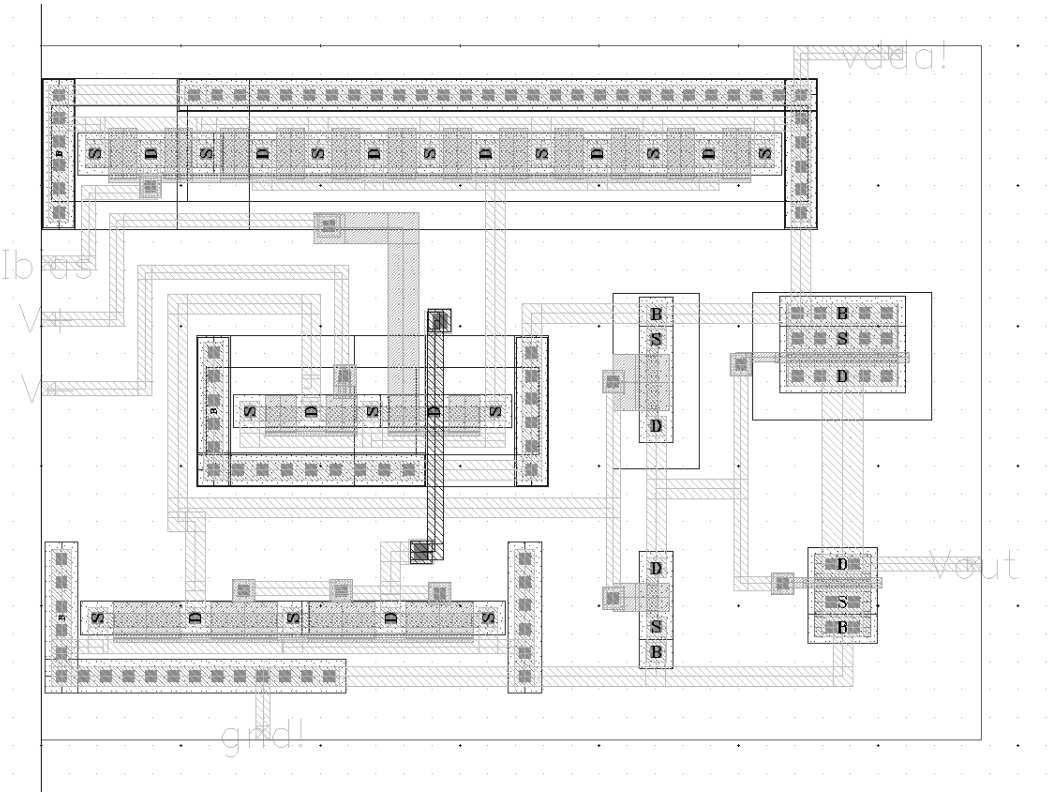

Figure B.7: Layout implementation of the PWM generation comparator as fabricated into the integrated circuit

The layout of the PWM generation comparator is shown in Figure B.7. This circuit consists of a current mirror, differential pair and two inverters increasing in size to act as a buffer to be capable of charging and discharging the gate capacitance of the two switching devices of the Dual Boost converter at 200 kHz.

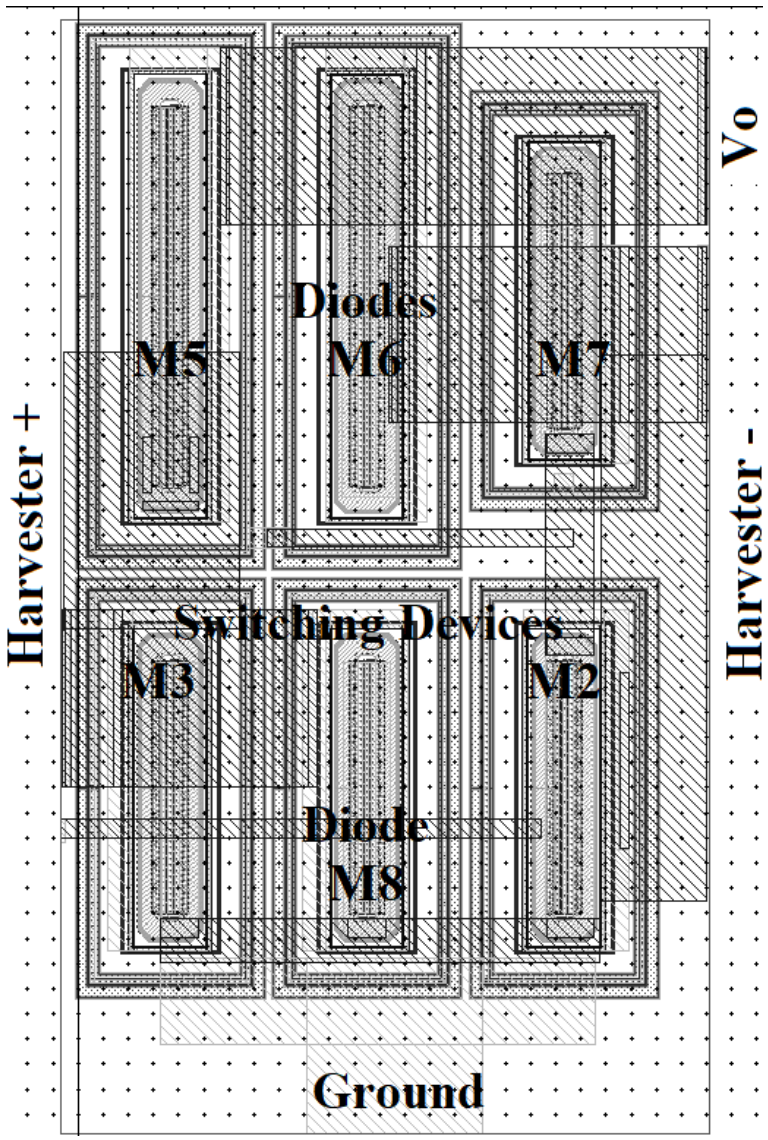

Figure B.8: Layout implementation of the AC/DC-to-DC Improved Dual Boost converter as fabricated into the integrated circuit

The layout of the dual boost converter is shown in Figure B.8. All the transistors are high voltage transistors with thinnest gate oxide available in the technology NMOS50IT. Transistors *M5*, *M6*, *M7* and *M8* are diode connected transistors and operate as diodes. *M5* and *M6* are the usual diodes which are an essential part of the Boost converters. *M7* and *M8* are diodes to bypass the parasitic diodes of the switching devices for the converter to obtain better efficiency levels. The

switching devices are transistors *M2* and *M3*. Particular attention was given to all metal interconnects and vias so that the converter is capable to operate at currents of up to 26 mA. According to [94], Metal 1 and Metal 2 layers have a current density of 0.67 mA/µm. Hence all high current metal interconnects in the dual boost converter are 40 µm wide. Gate metal interconnects are 5 µm wide which can conduct an average current of 3.4 mA. The total gate capacitance of the two switching devices *M2* and *M3* is 20 fF. The average current necessary to charge and discharge this capacitance to 2 V at a switching frequency of 200 kHz is negligible. Although the gate metal interconnects are wider than necessary in terms of the metal interconnect current density, to reduce the transistor switching losses, the gates need to discharge and charge in the shortest time possible. Widening the metal interconnects decreases the resistance, which switches on and off the transistors faster.

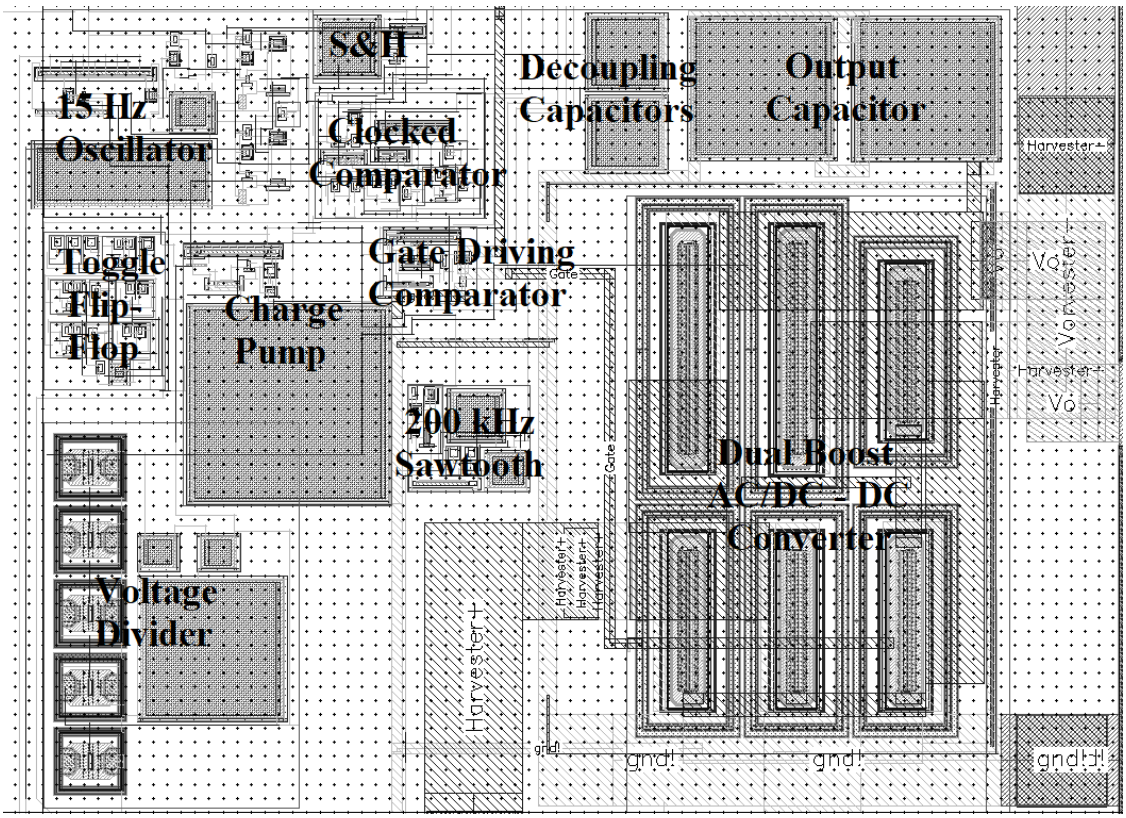

Figure B.9: Layout implementation of all blocks as fabricated into the integrated circuit

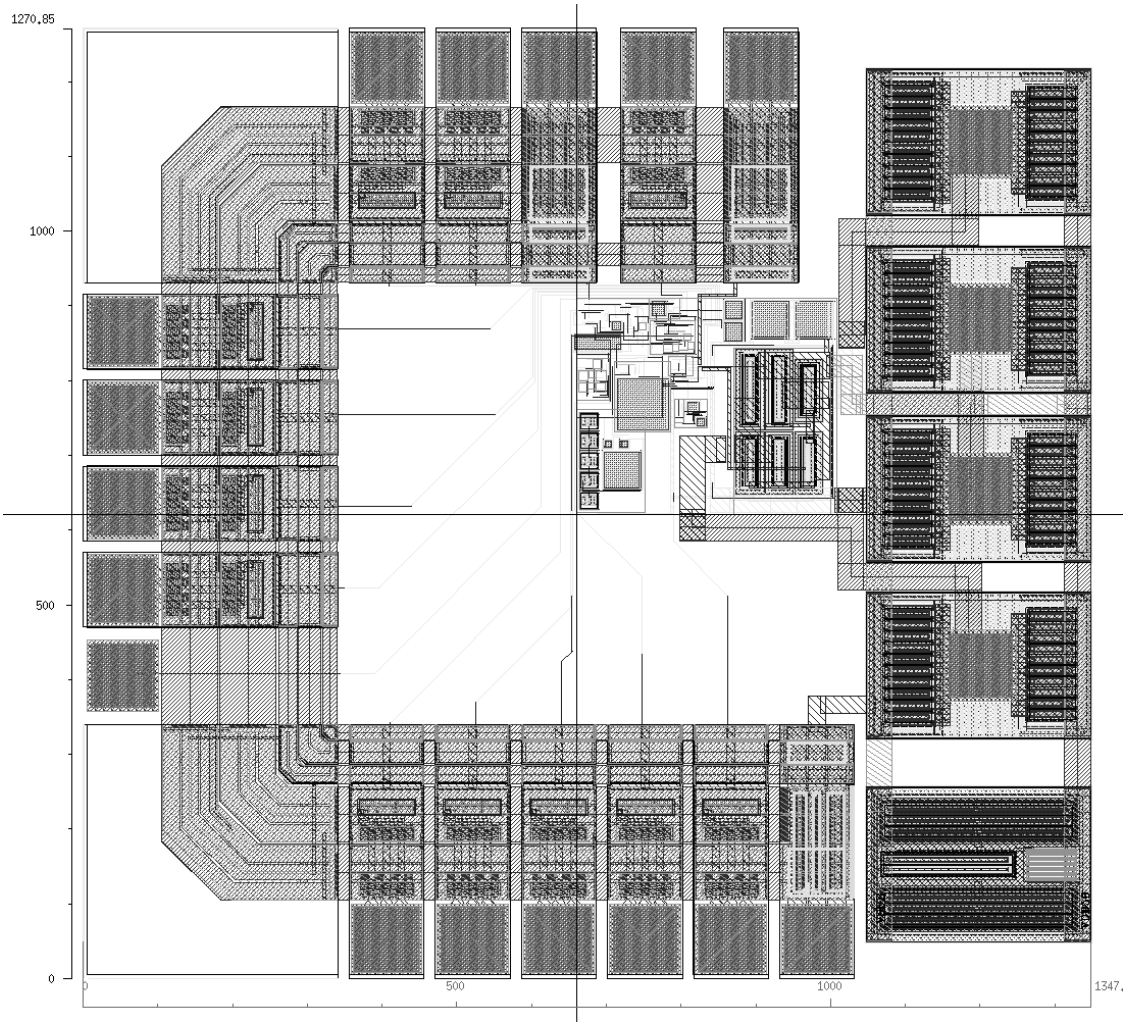

Figure B.10: Layout implementation of all the blocks and pads as fabricated into the integrated circuit

The dimensions of the integrated circuit including the pads are 1271 µm by 1347 µm, that is an area of 1.7 mm^2. Post-layout simulations including the pad loading were carried out. Since this circuit is being fabricated as a prototype, pads were included for every input and output in every block so that the operation of all the circuits individually can be monitored externally. Although this is a good approach for prototyping and testing, pad loading increases the power consumption of the circuits especially those working at a high frequency and slows the response time of the circuits. In fact, the post-layout simulations are essential especially in this

circuit due to the very low currents involved. Consequently, pad loading can have adverse effects on the circuit's operation. Post-layout simulations proved successful, and the pad loading did not affect the circuit's correct operation.