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Considerations on the Development of High-Power Density Inverters for Highly Integrated Motor Drives

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Abstract: In transportation electrification, power modules are considered the best choice for power switches to build a high-power inverter. Recently, several studies have presented prototypes that use parallel discrete MOSFETs and show similar overall output capabilities. This paper aims to compare the maximum output power and losses of inverters with different types (surface-mounted, through-hole-mounted and power modules) of commercially available switching devices, and, therefore, discuss the theoretical boundaries of each technology. The numerical analysis relies on detailed power loss and thermal models, with adjustments made for gate current and realistic parameters of the cooling system. The analysis includes two case studies with different targets, including minimum dimensional characteristics and maximum output power. The results demonstrate that discrete MOSFETs can provide improved capabilities in contrast to power modules under certain conditions.

Keywords: three-phase inverter; parallel MOSFETs; silicon carbide (SiC)

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1. Introduction

An electrical drive is a sub-system on which significant efforts are pushed towards the electrification of transportation, and its crucial role is known throughout all sectors of industry. As a result, electrical drives are able to compete with internal combustion engines or gear transmission systems in terms of operational values. While electric drive technology has made remarkable steps forward in the last few decades, many challenges remain. These include the implementation of new functionalities, higher power density and system reliability and better components availability [1]. The concept of motor integration is one of the central themes to all the above. To achieve higher system operational requirements, the physically integrated approach coupled with higher speeds and new materials is critical [2]. Moreover, industry-oriented studies [3,4] have stated that harsh operating conditions may introduce further technical challenges for electrical drivers in some Electric Vehicle (EV) applications.

The development of a power converter for an integrated motor drive with an output power ranging from several dozens to hundreds of kW often requires moving away from traditional patterns and using unconventional design methods. Several distinct approaches are used to achieve the desired power level. A group of researchers applied custom-designed power modules to avoid the temperature limitations of the package's materials [5–7]. Such modules use a ceramic substrate and silicon carbide (SiC) dies without a plastic cover; therefore, the maximum temperature is limited only by the thermal capability of the SiC, solder and a baseplate. A clear disadvantage of this approach is that the exploitation of the design in research or industry is difficult, and complicated equipment is required to produce custom SiC modules. Researchers do have to choose the serially produced SiC products in order to obtain a converter that can be repeated or manufactured.

Another approach commonly used to achieve the required power is to exploit commercial SiC power modules [8–12], as they are featured with the best thermal performance and a high current rating among other serially produced components. Power modules are

convenient and effective means of building a power converter. On the other hand, their heavy weight and bulky dimensions (see Figure 1) might cause difficulties with the layout if the project demands a specific complex housing shape.

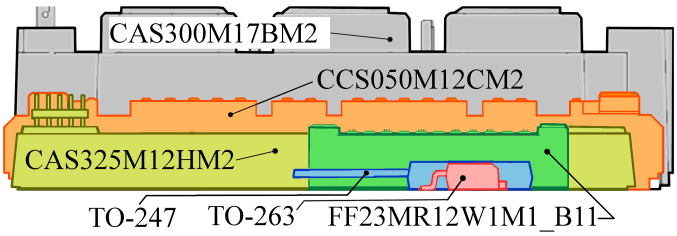

Figure 1. Different packages of SiC MOSFETs [13].

The maintenance and modernization of the converter with power modules might also be challenging due to the large variety of their shapes and terminal locations; examples of modules are shown in Figure 2. The transition to other series or manufacturers of power modules mostly causes the redesign of the inverter's other components.

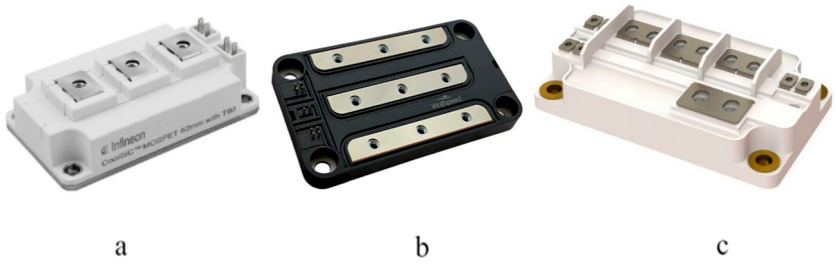

Figure 2. Power modules with different terminal locations: (**a**)—Infineon CoolSiC module [14]; (**b**)—Wolfspeed HM3 module [15]; (**c**)—microchip power module [16].

Alternative power electronics designs based on discrete components can provide an optimal solution with higher flexibility to operate a variety of standardized power switching devices. A number of studies [17–21] demonstrated that high power inverters with parallel SiC MOSFETs can prove their competitiveness in this application field. However, it remains unclear what the possible output current and power that discrete components can reach, as many factors may affect the performance.

This paper aims to demonstrate the capabilities of power modules and through-hole (THT) and surface-mounted (SMT) discrete SiC MOSFETs under the same operating conditions across a range of ambient/cooling temperatures. The results might assist engineers and researchers to obtain a more comprehensive picture of theoretical power boundaries and features of different MOSFET packages. A thermal model with a losses analysis utilizes datasheet information about temperature and drain current-dependent parameters to obtain accurate results. A large number of publications (for instance, [22–24]) have applied a losses thermal model for the needs of optimization within a single design or topology comparison. However, these papers did not cover many MOSFET types and did not focus on the evaluation of maximum output power. Moreover, this study considers the external gate resistance as an input parameter for analysis due to the limitation of the gate driver's output current. In order to address the interests of integration-oriented studies, the analysis also includes occupied area, mass and volume parameters to assess the effect of different packages on the dimensions and weight of the inverter.

The rest of the paper is organized as follows. Section 2 describes the proposed thermal model and selection criteria of MOSFETs, while Section 3 demonstrates the analysis of the first case study with a fixed output power. The results of the second case study with maximum output power are mentioned in Section 4, which is followed by the discussion in Section 5.

2. Materials and Methods

2.1. Power Switches

Three package types of semiconductor power switches were examined in this study as a potential choice for the role of the Integrated Motor Drive (IMD) power switch.

2.1.1. Discrete SiC MOSFETs

SiC MOSFETs are presented on the market in a large variety of drain current capabilities and blocking voltages to help designers balance between performance, power losses and economic reasonability. Several manufacturers of SiC MOSFET in SMT and THT packages have started production since its first appearance in the mid-2010s. Devices with the best figures for the drain current are included in the analysis to demonstrate the best achievable capabilities. Maximum blocking drain voltage of selected MOSFETs does not exceed 1200 V to target typical requirements for typical aircraft bus voltage and EV traction drivers.

In detail, important characteristics of many up-to-date commercially available SMT SiC MOSFETs are presented in Table A1. Although TO-263-7 is the oldest and the most popular package type, developers introduce smaller packages to reduce height and the chip area targeting embedded electronics and highly integrated solutions.

All THT MOSFETs have TO-247-4 package (or its variants) due to reduced power losses by comparison with the earlier 3-pin design of TO-247, where the gate driver circuit uses the source pin. In total, 9 types by 7 companies were selected, and their parameters are presented in Table A2.

The production of SiC MOSFETs is an active and dynamically developing industry with both gradual enhancement of existing technologies and the testing of new approaches. Updated versions of semiconductor devices emerge regularly and extend the performance boundaries of power electronics.

2.1.2. Power Modules

Power modules contain semiconductor switching devices with large die areas or parallel dies to achieve high values for output current and level up power density. Advanced technological processes enable the utilization of materials with thermal conductivity while standardized procedures maintain the repeatability of characteristics and predictable reliability.

The parallel connection of semiconductor power modules in a single switching unit is not a common practice due to difficulties with current sharing and stability without additional measures. Relatively large distances between terminals lead to high inductances in gate traces and high-power buses and, therefore, disturbance of gate signals and current inequality. Detailed parameters of power modules included in the consideration are listed in Table A3.

2.2. Losses Calculation and Thermal Model

If high-power density is the primary goal, power electronics designers must operate power switches at the maximum of their thermal capabilities. Maintaining the junction temperature below the rated value requires careful evaluation of the MOSFET's operating point and heat dissipation. In order to minimize weight and dimensions, the number of MOSFETs should be kept to a minimum.

Some assumptions were made to simplify the calculations:

- All parallel devices share phase drain current in equal parts;
- Dead-time-related losses (difference in conduction losses between diodes and MOSFETs) were not included;
- Diode partial current sharing in 3rd quadrant was not considered in this model; therefore, diode's conduction losses were not included in calculations.

Maximum and RMS drain currents of a device ($I_{DS\ max}$ and $I_{\mathrm{DS}rms}$ respectively) were calculated as follows:

$$I_{\mathrm{DS}\ rms} = \frac{I_{\mathrm{GR}\ rms}}{N_{PPG}} = \frac{I_{\mathrm{PH}\ max}}{2N_{PPG}},\ I_{DS\ max} = \frac{I_{\mathrm{PH}\ max}}{N_{PPG}} \tag{1}$$

where N_{PPG} is the number of devices per group, $I_{\mathrm{GR}\ rms}$ is the group RMS current and $I_{\mathrm{PH}\ max}$ is the maximum phase current.

The power losses of a MOSFET (P_{MOSFET}) are calculated as the sum of conduction (P_C) and switching power losses (P_{SW}). Considering sine PWM modulation, switching losses can be expressed through their maximum value of a cycle:

$$P_{MOSFET} = P_C + P_{SW} = I^2_{\mathrm{DS}\ rms} \cdot R_{ds\ on}\left(T_J, I_{DS\ max}\right) + F_{sw}\frac{E_{SW\ tot\ rated}}{\pi} K_{TJ} \cdot K_{VDC} \cdot K_{IDS} \cdot K_{RG} \tag{2}$$

where $E_{SW\ totrated}$ is the total switching losses under the rated conditions that are specified in the datasheet, K_{TJ} is the junction temperature (T_J) scaling coefficient, K_{VDC} is the input DC-link voltage (V_{dc}) scaling coefficient, K_{IDS} is the maximum drain current ($I_{DS\ max}$) scaling coefficient and K_{RG} is the scaling coefficient of gate external resistance ($R_{g\ ext}$). Parameters, measured or specified at the rated operating point (selected by manufacturer for the measurement of switching energy losses), have an index "rated" in their description. Reverse recovery losses are already included in total switching losses because manufacturers use the same type of MOSFET as a body diode to obtain experimental values specified in the datasheet.

In the calculation model the drain-source channel resistance $R_{ds\ on}$ depends on T_J and $I_{DS\ max}$:

$$\begin{gathered} R_{ds\ on}\left(T_J,\ I_{DS\ max}\right) = R_{ds\ on25}\left(1 + K_{RTJ}\left(T_J - T_{J\ LT}\right)\right) \cdot K_{RI}(I_{DS\ max}) \\ K_{RTJ} = \frac{Rn_{ds\ on\ TJ\ HT} - 1}{T_{J\ HT} - T_{J\ LT}},\ K_{RI}(I_{DS\ max}) = \frac{A_{RI} \cdot I_{DS\ max} + B_{RI}}{R_{ds\ on25}} \end{gathered} \tag{3}$$

where $R_{ds\ on25}$ is the drain-source channel resistance at 25 °C, $Rn_{ds\ on\ TJ\ HT}$ is the normalized value (divided by $R_{ds\ on25}$) of MOSFET active resistance under high temperature $T_{J\ HT} = T_{J\ max}$ and $T_{J\ LT}$ is the maximum junction temperature, where $R_{ds\ on}$ is close to $R_{ds\ on25}$. Values of A_{RI} and B_{RI} are obtained at the datasheet for the current range 20 A–70 A using linear approximation with acceptable error. Polynomial approximation might be used to follow the non-linear curve for higher drain current.

The shapes of the curves for different parameters vary significantly, so linear, quadratic and power approximations were selected to calculate coefficients:

$$\begin{gathered} K_{VDC}(V_{DC}) = \left(\frac{V_{DC}}{V_{DC\ rated}}\right)^{A_{VDC}};\ K_{IDS}(I_{DS\ max}) = \frac{A_{IDS} \cdot {I_{DS\ max}}^2 + B_{IDS} \cdot I_{DS\ max} + C_{IDS}}{E_{SW\ tot\ rated}}. \\ K_{TJ}(T_J) = \frac{A_{TJ} \cdot T_J + B_{TJ}}{E_{SW\ tot\ rated}},\quad K_{RG}(R_{g\ ext}) = \frac{A_{RG} \cdot R_{g\ ext} + B_{RG}}{E_{SW\ tot\ rated}}, \end{gathered} \tag{4}$$

where A_x, B_x and C_x are parameters extracted from MOSFET's datasheet.

In single MOSFET operations, a gate driver's output current does not affect the performance of MOSFET due to the high current capabilities of recently developed gate drivers. The most popular maximum value of the output current for a single chip is approximately 30 A, so this value was also the maximum total gate current for analysis. In the analysis t_{rise} (target value is 20 ns) determines the initial value of $R_{g\ ext}$ as it might be important for Electromagnetic Interference (EMI) characteristics of the inverter [25], although gate driver current might be used as an input parameter. At the same time, the possible minimum value $R_{g\ ext\ min}$ in the analysis was determined using the minimum value of $R_{g\ ext}$ mentioned in datasheet to increase accuracy of calculations.

The relationship between the total maximum gate current I_{GTotal} and the number of parallel transistors can be expressed as follows:

$$I_{Gtotal} = N_{PPG}\frac{V_{GDMax} - V_{GDMin}}{R_{g\ inner} + R_{g\ ext}} \leq 30\ \text{A} \tag{5}$$

Total gate current I_{Gtotal} increases with the number of parallel devices in a group and might reach the limit at some point. Further increase in the number of devices leads to an increase in gate resistance $R_{g\ ext}$ in order to maintain the current at the same level.

For some devices, high inner resistance $R_{g\ inner}$ and significant value of gate-drain charge Q_{gd} does not allow a driver to charge C_{gd} fast enough to reach the initial value of t_{rise}. For such devices, the initial value of external gate resistance $R_{g\ ext}$ is set to $R_{g\ ext\ min}$. Thus, external resistor $R_{g\ ext}$ for each group of MOSFETs was calculated with respect to the value of gate current:

$$R_{g\ ext} = \begin{cases} N_{PPG}\frac{V_{GDMax}-V_{GDMin}}{I_{GtotalMAX}} - R_{g\ inner}, & if\ I_{Gtotal} = 30\ \text{A} \\ \frac{t_{rise}\ (V_{GDMax}-V_{GDMill})}{Q_{gd}} - R_{g\ inner}, & if\ I_{Gtotal} < 30\ \text{A} \\ R_{g\ ext\ min}, if\ \ I_{Gtotal} < 30\ \text{A}\ and\ \frac{t_{rise}\ (V_{GDMax}-V_{GDMill})}{Q_{gd}} < R_{g\ inner} \\ R_{g\ ext\ min}, & if\ R_{g\ ext\ min} > R_{g\ ext} \end{cases} \tag{6}$$

The final value $R_{g\ ext}$ was used to calculate the coefficient K_{RG} for switching losses.

Although datasheets for most modern MOSFETs contain all the necessary information, documents for older MOSFETs might miss some plots or figures. In that case, default values selected using simplified losses equations were used in the calculation (values are listed in Table 1).

Table 1. Default values of coefficients for losses calculation.

Coefficient Name	Equation's Parameters' Default Values	Coefficient Default Value
K_{RG}	Not applicable	$\frac{R_{g\ ext}+R_{g\ inner}}{R_{g\ ext\ rated}+R_{g\ inner}}$
K_{TJ}	$A_{TJ} = 0$, $B_{TJ} = E_{SW\ tot\ rated}$	1
K_{VDC}	$A_{VDC} = 1.4$	$\left(\frac{V_{DC}}{V_{DCrated}}\right)^{1.4}$
K_{IDS}	$A_{IDS} = C_{IDS} = 0$, $B_{IDS} = \frac{E_{SW\ tot\ rated}}{I_{DS\ max\ rated}}$	$\frac{I_{DS\ max}}{I_{DS\ max\ rated}}$
K_{RTJ}	$Rn_{ds\ on\ TJ\ HT} = 1$	0
K_{RI}	$A_{RI} = 0$, $B_{RI} = R_{ds\ on25}$	1

The junction temperature of a device consists of the ambient temperature T_{amb}, temperature drop between MOSFET's case and junction ΔT_{j-case} and temperature drop between the case and coolant $\Delta T_{case-hs}$:

$$T_j = \Delta T_{case-hs} + \Delta T_{j-case} + T_{amb} = P_{MOSFET}\left(\Theta_{j-c} + \Theta_{c-hs} + \frac{1}{S_{PCBAREA}h_{CP}}\right) + T_{amb},$$
$$\Theta_{c-hs} = \begin{cases} \Theta_{TIM}, & for\ power\ modules \\ \Theta_{Insulation\ pad} + \Theta_{TIM}, & for\ THT\ components \\ \Theta_{PCB} + \Theta_{TIM}, & for\ SMT\ components \end{cases} \tag{7}$$

where S_{hs} is the area of the thermal pad or the baseplate of a device divided by the number of switching groups inside the package (assuming that heat evenly spreads across the baseplate) and Θ_{c-hs} is the total thermal resistance of layers between the case and the heat sink. A traditional structure with indirect cooling of power modules was selected for comparison analysis. The thermal model of THT components implies that heat is transferred through a thermally conductive insulation pad (mica + thermal grease), and

for SMT components Insulated Metal Substrate (IMS) was selected as a reference for Θ_{c-hs} values with Printed Circuit Board (PCB) and Thermal Interface Material (TIM) parameters.

As the inverter's area is one of the targets, keeping a small distance between devices was reasonable. For analysis, the distance between two MOSFETs was 2 mm, and each device used an extra 1 mm layer of copper on each side of its thermal pad to spread the heat. Other important parameters of thermal interface materials and calculated values of MOSFET's thermal resistances are stated in Table 2.

Table 2. Thermal resistances of the utilized calculation model.

Input Parameter	Device Type	Value	Calculated Parameter	Device Type	Value
Prepreg thickness, mm	SMT	0.1	Junction–ambient thermal resistance θ_{single}(per MOSFET), K/W	SMT	2.66–4
Prepreg thermal conductivity, W/m·K		1			
Top copper layer thickness, mm		0.07			
Insulation (mica + grease) thermal resistance per area, K/cm^2·K	THT	0.65	Junction–ambient thermal resistance θ_{single}(per MOSFET), K/W	THT	0.88–1.05
Heat sink area per a MOSFET (for SMT and THT), mm^2	SMT/THT	(L + 10)·(W + 2)	Junction–ambient thermal resistance θ_{single}(per MOSFET), K/W	power modules	0.148−0.54
Grease thermal conductivity, W/m·K	SMT/THT/Modules	0.73			
Heatsink heat transfer coefficient, W/cm^2·K		0.5			

L, W—length and width of MOSFET's case.

The volume (V) and the area (A) of a power module were calculated based on their dimensions from datasheets. The area and the volume of SMT and THT devices included extra space (values are presented in Figure 3) for connections of power buses and gate circuits:

$$A_{SMT} = 6(N_{PPG}(Width + 2\text{ mm}) + 2\text{ mm})(Length + 10\text{ mm}), \quad (8)$$

$$A_{THT} = 6(N_{PPG}(Width + 2\text{ mm}) + 2\text{ mm})(Length + 10\text{ mm}), \quad (9)$$

$$V_{SMT} = A_{SMT}(Height + 7\text{ mm} + 2\text{ mm}),\ V_{PTH} = A_{PTH}(Height + 7\text{ mm}) \quad (10)$$

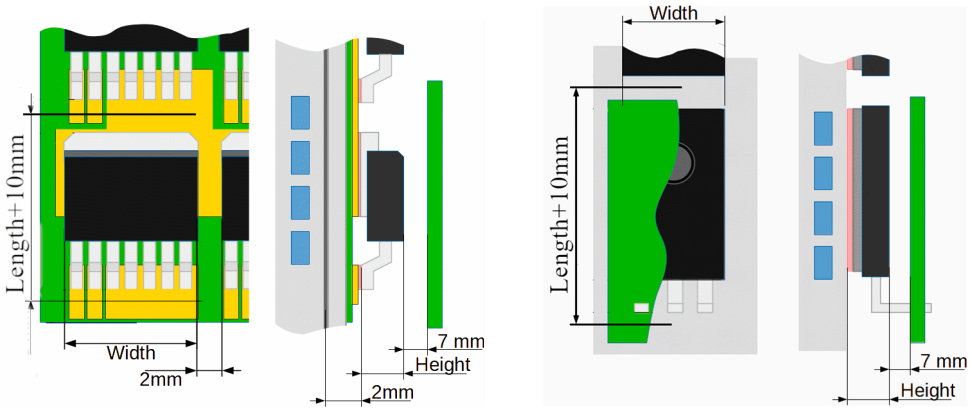

Figure 3. Layout for SMT (TO-263-7) and THT (TO-247) components.

The high junction temperature T_j affects many parameters of MOSFET and causes an increase in both conduction and switching losses, which, in turn, increase the generated heat and junction temperature. A multi-iteration algorithm was used to recalculate temperature-dependent coefficients and obtain accurate results for the whole range of junction temperature (see Figure 4). The initial junction temperature was equal to the coolant temperature and was updated every cycle until the difference between the two steps is less than 2 °C. This method helped to detect possible thermal runaway and evade overestimation of conductive losses due to too high expectation of $R_{ds\ on}$. All combinations that led to excessive junction temperature were excluded from the analysis.

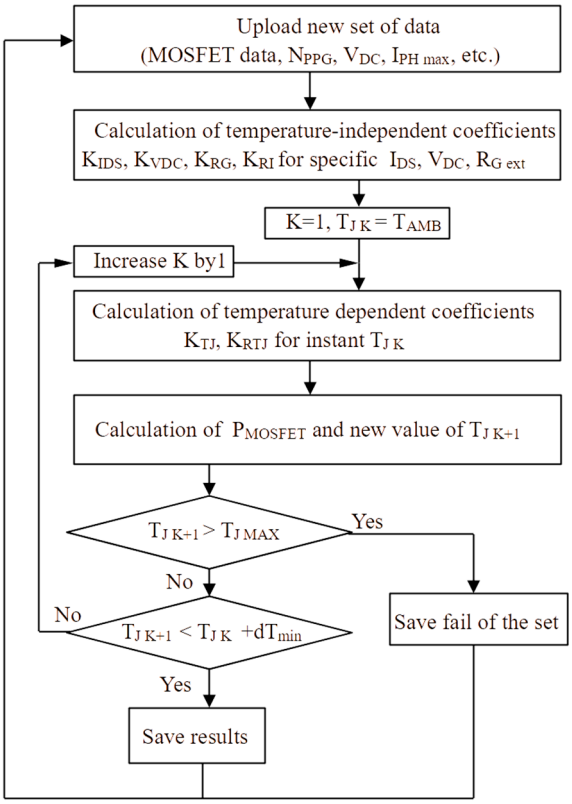

Figure 4. Flowchart for the calculation of junction temperature.

The total weight W_{SMT} of an inverter with SMT components includes the weight of a 2 mm aluminum baseboard as they cannot be used without a heat spreader and can be calculated as

$$W_{SMT} = 6N_{PPG}W_{part} + A_{SMT} \cdot 0.2 \text{ cm} \cdot 2.7 \frac{\text{g}}{\text{cm}^2} \quad (11)$$

where W_{part} is the weight of the single discrete element according to its datasheet.

3. Performance Analysis

3.1. Effect of Gate Driver Current in Parallel Connection

All calculations were performed in MATLAB software package (version R2022b Update 3).

The results for the gate current analysis are presented in Figure 5 (for SMT MOSFETs), Figure 6 (for THT MOSFETs) and Figure 7 (for power modules). Different behaviors of $R_{g\ ext}$ could be noticed with a current limitation ($R_{g\ ext}$ changed with the increase in N_{PPG}) and without a current limitation ($R_{g\ ext}$ was constant).

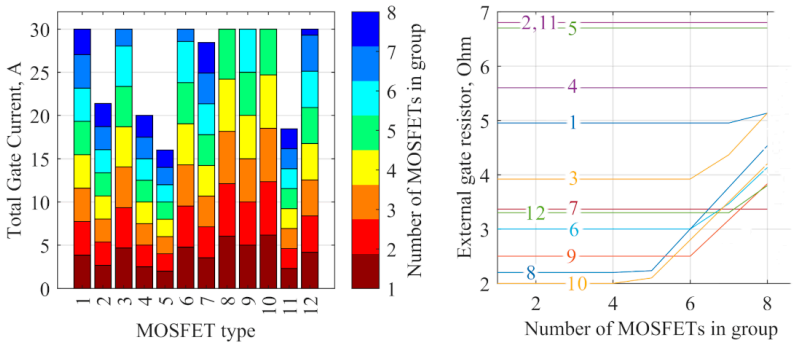

Figure 5. Total gate current and external gate resistance of SMT MOSFETs.

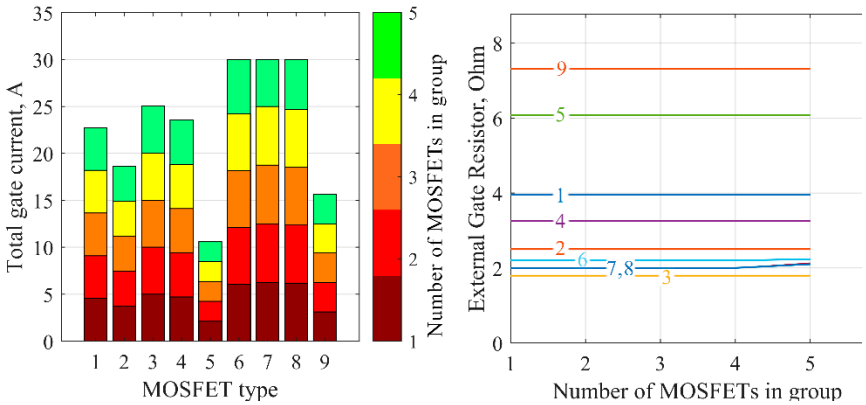

Figure 6. Total gate current and external gate resistance of THT MOSFETs.

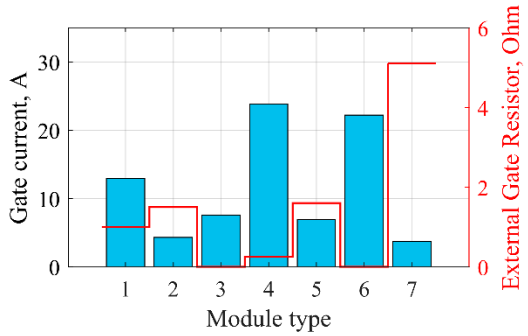

Figure 7. Total gate current and external gate resistance of power modules.

The maximum number of parallel devices was set to 8 for SMT MOSFETs and 5 for THT MOSFETs.

The THT MOSFETs showed almost the same pattern with the only difference that fewer devices reached the maximum gate current threshold due to the lower number of devices per group.

The power modules showed a wide variety of results in terms of gate current, but relatively high inner and minimum external resistances limited the switching capabilities significantly, so no module could reach 30 A of gate current.

3.2. Case 1—Operation under Normal Ambient Temperature

This scenario included a detailed analysis of inverter operation under a normal ambient temperature of 25 °C. The system parameters used in the calculation are presented in Table 3; the values were chosen according to the requirements for a typical low-power IMD (for example, [26–28]). The discrete MOSFETs were connected in parallel and the number of devices per group was selected according to the device's calculated maximum junction temperature.

Table 3. IMD parameters for comparative analysis.

Parameter	Value
Peak phase current $I_{\mathrm{PH}\ max}$, A	200
DC voltage V_{DC}, V	400
Switching frequency F_{sw}, kHz	50
Coolant temperature T_{COOLANT}, °C	25
HTC of the cold plate h_{cp}, W/cm^2·K	0.5

Individual results for the different packages are presented in Figures 8–10. For discrete MOSFETs, two sets of data with a different number of parallel devices ($N_{PPG\ MIN}$ and

$N_{PPG\ MIN} + 1$) indicated the change in thermal conditions if the number of devices is increased to obtain a safety gap and reduce thermal stress. SMT devices showed the highest average junction temperature, with a significant drop (20–60 °C) in the junction temperature for the case of $N_{PPG\ MIN} + 1$.

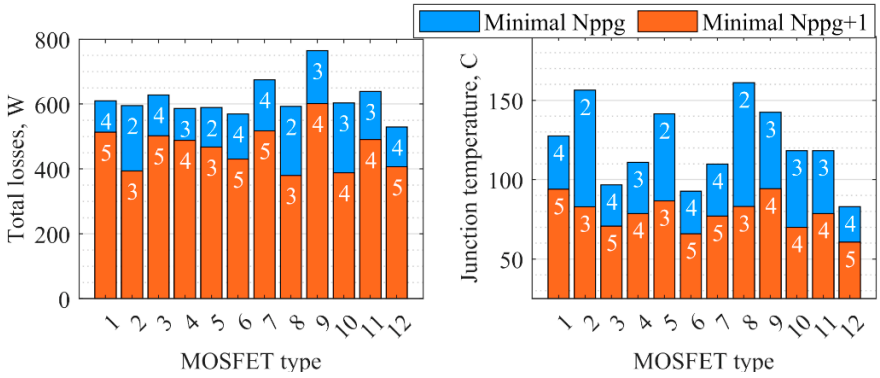

Figure 8. Total losses and junction temperature of SMT MOSFETs in Scenario 1 (T_{amb} = 25 °C).

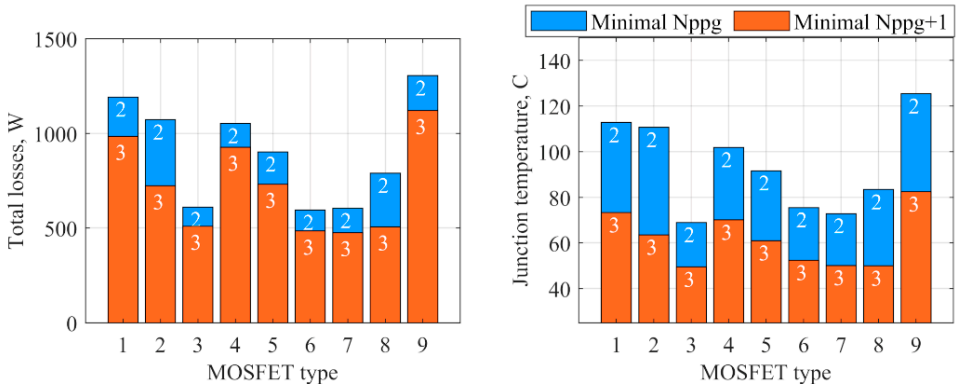

Figure 9. Total losses and junction temperature of THT MOSFETs in Scenario 1 (T_{amb} = 25 °C).

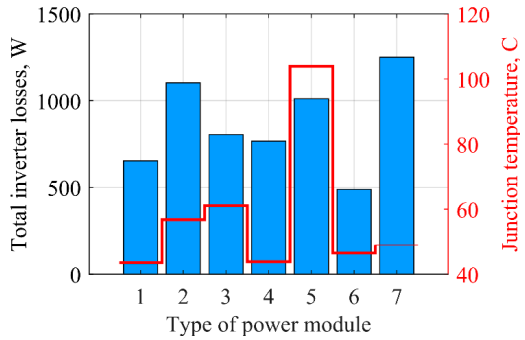

Figure 10. Total losses and junction temperature of power modules in Scenario 1 (T_{amb} = 25 °C).

The average junction temperature for THT devices was lower by approximately 30 °C than the value for SMT packages and decreased by another 20 °C for a larger group. All devices could achieve the required performance with only two devices per group, but the total losses showed higher values than for SMT devices.

Power modules showed the same level of total losses and, in general, low values for the junction temperature (presented in Figure 10). Although compact three-phase power modules (№5) had the highest junction temperature among other modules and average total losses for a given power level, the small package gives them an obvious advantage in applications with mass or volume restrictions.

It is worth mentioning that the analysis of an inverter's mechanical characteristics should not only consider the pure dimensions and weight of the semiconductor devices,

but should also include other components of the inverter. Otherwise, the comparison demonstrates overly optimistic results (reduction by 5–10 times) for discrete components that are difficult to obtain in real applications. Some additional values can be introduced to obtain adequate figures for the characteristics of the inverter (see Table 4).

Table 4. Additional values for dimensional analysis of the inverter.

Parameter	Area	Weight	Volume
Additional values	1.5 cm *	1.5 kg **	1.5 L **

*—to each side of a switching group (for screws, tolerance, etc.). **—that includes other components, a case and a heatsink, total power density is approximately 30 kW/L(or 30 kW/kg).

According to the calculations (see Figure 11), the inverter area and volume with their maximum numbers of MOSFETs were almost the same for both THT (package TO-247-4) and SMT devices (package TO-263-7). The different color areas for SMT and TO-247 show the number of parallel devices (from 1 to 8 for SMT, from 1 to 8 for TO-247). Different colors and corresponding numbers for modules indicate the exact type numbers.

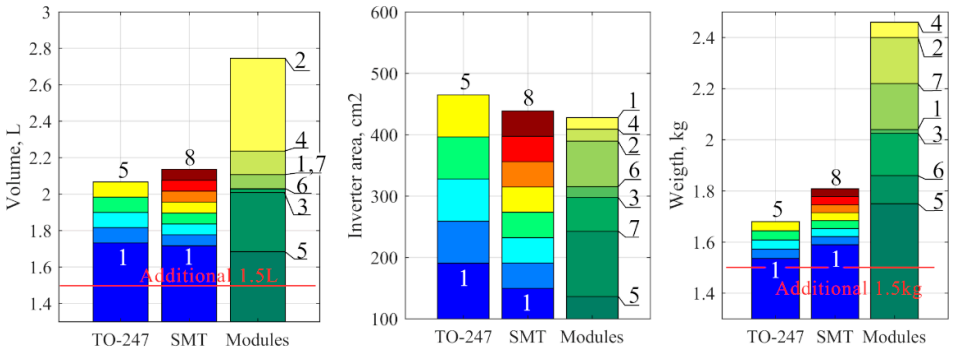

Figure 11. Results of dimension analysis (additional values are included).

Power modules showed significant deviations in dimensions and weight from the average level due to differences in the package design and ampacity. In fact, there was no significant difference in the inverter's area or volume between discrete components and power modules. Nevertheless, almost all options with modules were heavier than assemblies of discrete MOSFETs; therefore, discrete components are a better choice if the weight is a target parameter of the system design.

The radar diagrams in Figure 12 compare the obtained results between packages. The values were normalized using the maximum value among all types of devices for each comparative characteristic. The color area shows the range of values for all components from that group. Furthermore, the results for three MOSFETs from each package are shown to illustrate the relationship between parameters.

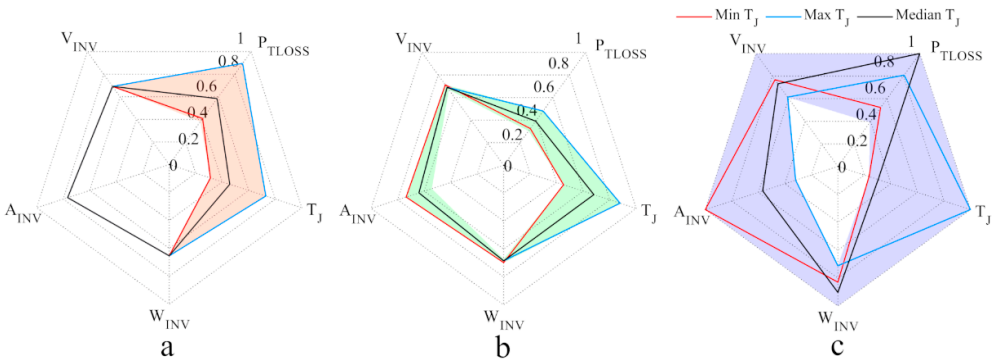

Figure 12. Normalized analysis results for the (minimum + 1) number of parallel devices T_{amb} = 25 °C ((**a**)—THT, (**b**)—SMT, (**c**)—power modules).

3.3. Case 1—Operation under High Ambient (Coolant) Temperature T_{amb} = 25–150 °C

The graph of the total losses and junction temperature as functions of ambient temperature (see Figure 13) for SMT devices shows the maximum ambient temperature for each type (vertical line and the number of MOSFET types). For most types, this temperature was between 140 °C and 150 °C for the given thermal properties of the PCB and the heatsink, and only two types could work at 150 °C or higher. In the plot, P (T_{amb}), the region shaded with red color, shows the maximum amount of heat that can be transferred from the board in the case of eight parallel MOSFETs with a surface temperature of 175 °C. The total MOSFET losses must stay below the red line to keep the junction temperature within the allowed region.

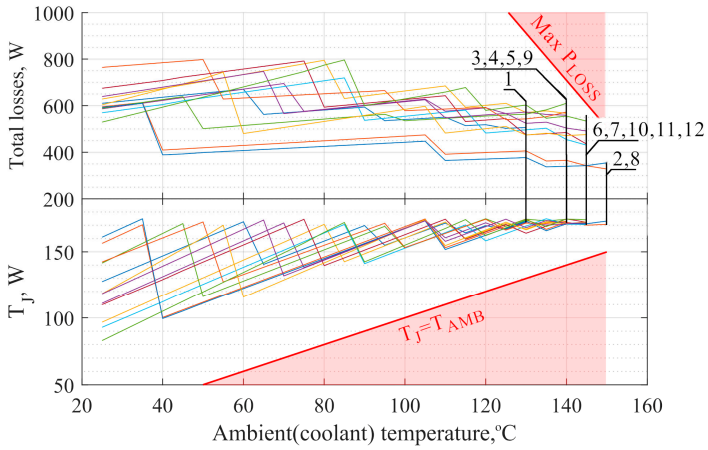

Figure 13. Total losses and junction temperature of SMT MOSFETs in Scenario 1 (Max P_{LOSS} represents the maximum heat that can be removed by an area of eight packages).

THT MOSFETs showed a better performance under harsh operating conditions, as four types could work within a specified temperature range (see Figure 14).

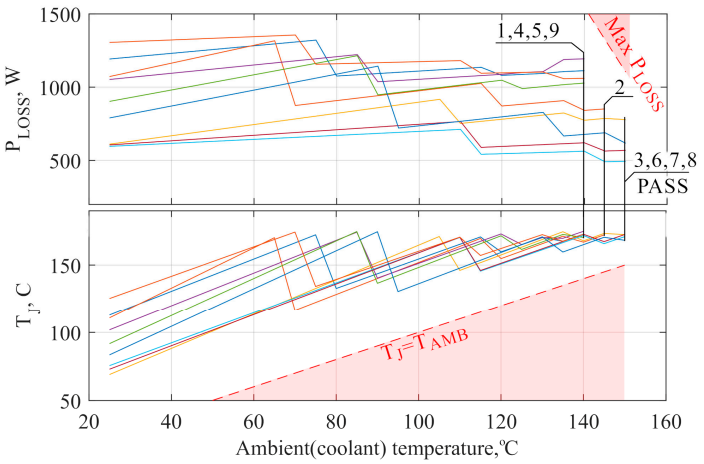

Figure 14. Total losses and junction temperature of THT MOSFETs in Scenario 1 (Max P_{LOSS} represents the maximum heat that can be removed by the total heatsink area).

The situation was different for power modules due to restrictions on the maximum case (baseplate) temperature. The absolute value is 125 °C for most devices, which might be a drawback for high temperature (HT) applications. The analysis results for power modules are shown in Figure 15.

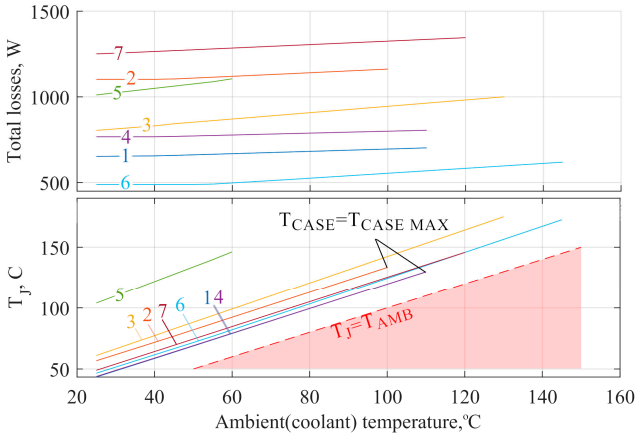

Figure 15. Total losses and junction temperature of power modules in Scenario 1 (T_{amb} = 25–150 °C).

3.4. Maximum Possible Output Power and Individual DC-Link Voltage (Case 2)

All devices operated at the absolute maximum of their junction temperature T_J and the number of parallel devices (for discrete MOSFETs) was set to the maximum so the highest output power could be achieved. In real applications, it is impractical to operate at the absolute maximum of junction temperature. However, this approach can still highlight general trends, reveal issues, and helps to compare the performance of different devices in various operating conditions.

It is essential to mention that the DC-link voltage V_{DC} was different for different MOSFETs and equal to $0.7 \cdot V_{DC\ max}$; therefore, a higher maximum blocking voltage helped reaching top figures in output power. An indicator of the DC-link voltage V_{DC} (high or low level) is provided in the maximum phase current plot above the MOSFETs' bars.

The results of the performance analysis under the normal ambient temperature of all packages are presented in Figure 16 including plots for total losses, maximum phase current and maximum output power. The number of devices is mentioned on the x-axis (SMT-first, power module-last). As expected, devices with 600 V blocking voltage showed a higher maximum phase current than 1200 V devices; however, their output power was still below the results of high voltage competitors. Although new SMT packages (PowerFLAT 8 × 8 HV №1 and H−PSOF8L №7) cannot deliver high output power, they can commutate decent output phase current and, therefore, be useful in height-limited applications (package height is 0.8 mm and 2.3 mm, respectively, against 4.5 mm for TO-263-7). THT MOSFETs demonstrated a higher output power (up to 400 kW) at the expense of an increase in total losses (more than 4 kW in average). Similar to SMT MOSFETs, TO-247 devices with lower $V_{DS\ max}$ reached a higher current, but the dominant role in maximum output power belonged to 1200 V MOSFETs. Due to the significant deviation in characteristics, power modules showed a wide range in both power losses and maximum output power; nevertheless, most modules could deliver 200–250 kW. The inverter's power losses followed the distribution of output power with maximum values for power modules and THT MOSFETs. At the same time, the maximum phase current was almost the same for all packages; therefore, all packages might be used in applications with limited DC link voltage (<450 V) and a high phase current.

The mediocre performance of power modules in the analysis can be explained by the underrating of the heat sink's efficiency (low heat transfer coefficient). The selected parameters of cooling system provided enough thermal conductivity for SMT and THT devices, as the influence of PCB or insulation layer is significant in the total thermal conductivity. By contrast, the combined thermal resistance of a power module and thermal grease is comparable with the resistance of the heat sink, limiting the potentially high performance of power modules. A higher flow rate of coolant or more sophisticated structure can increase the efficiency and, therefore, the power module's figures (see Figure 17).

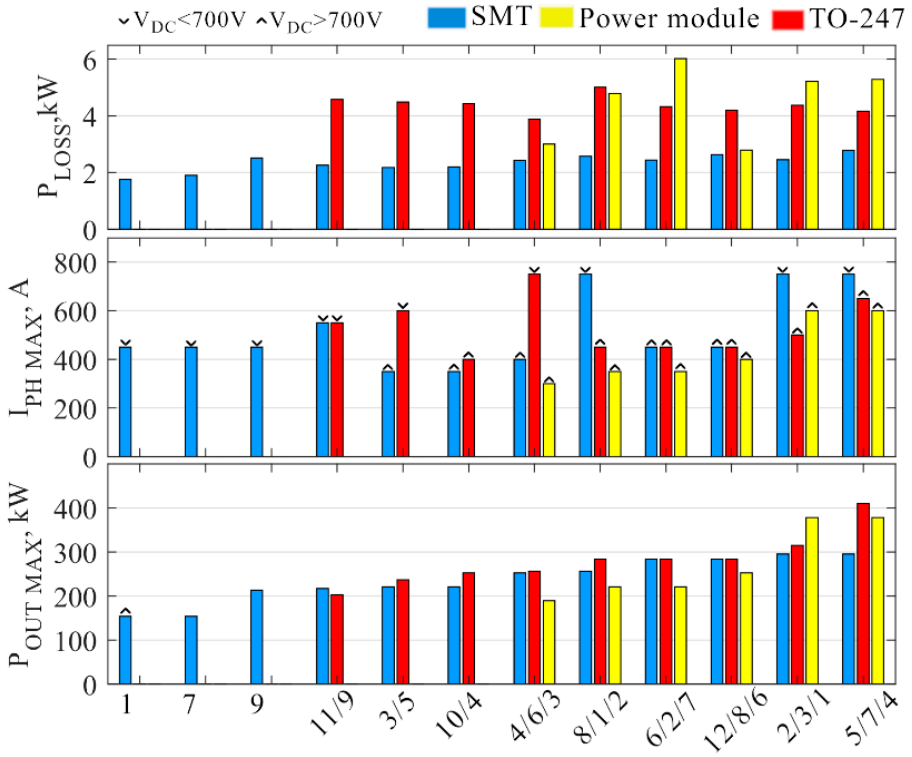

Figure 16. Simulation results of MOSFETs with maximum output power T_{amb} = 25 °C.

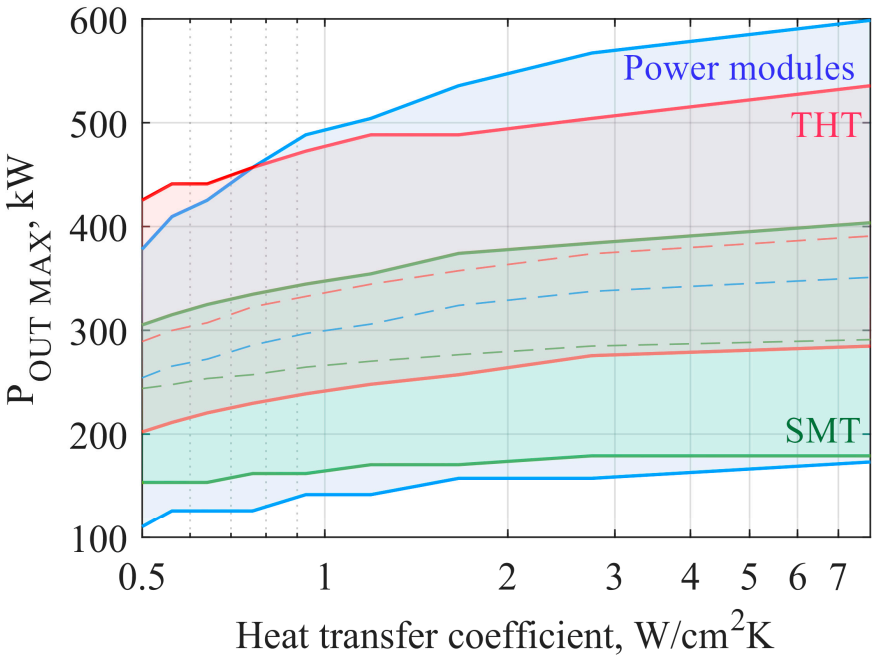

Figure 17. Ranges of maximum output power (all devices are included) for different packages under normal ambient temperature T_{amb} = 25 °C and various efficiency of the cooling system.

Graphs $P_{OUT}(T_{amb})$ for each power device from all three package types demonstrated a derating in output power with an increase in ambient temperature (see Figure 18). SMT and THT devices experienced an almost linear reduction in output power from 200–300 kW at 25 °C to less than 100 kW at 150 °C.

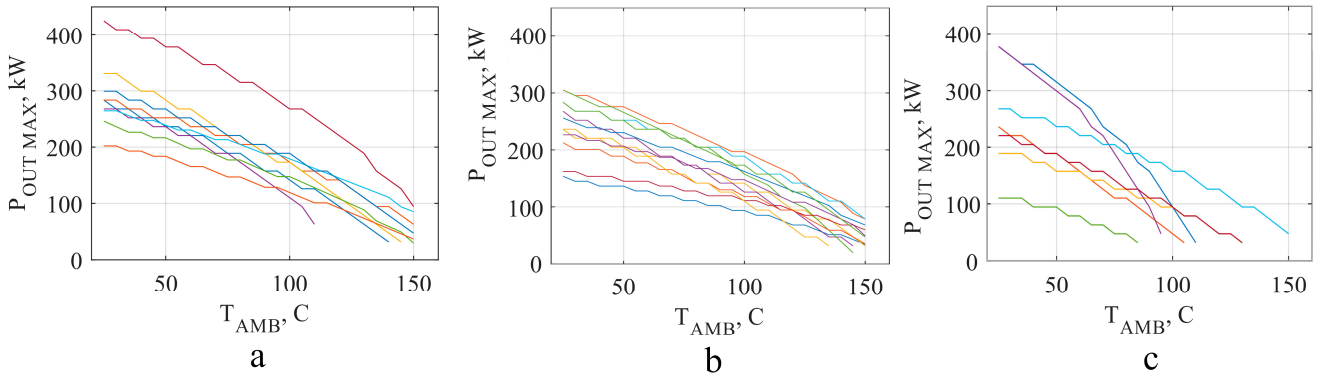

Figure 18. Maximum output power for THT (**a**), SMT (**b**) and power modules (**c**) devices within the range T_{amb} = 25–150 °C.

Although some modules demonstrated excellent results at a normal ambient temperature, they had higher rates of power reduction due to limited T_{CASE} as mentioned before. Power modules without case temperature restrictions showed better results, for example, GE12047CCA3. This module, similar to discrete elements, was limited only by the junction temperature, giving more freedom for a temperature distribution between junction and case points. Moreover, it had a small negative coefficient $dE_{SW}(dT_J)$ that maintained its switching losses almost at the same level within a whole range of operating temperature.

4. Experimental Validation

A three-phase two-level inverter was selected to validate the proposed thermal model of power devices' operating conditions. The switching group of the inverter included a single SiC MOSFET C2M0080120D connected to an air-cooled heat sink. The testing conditions and system characteristics are summarized in Table 5 and some components of test inverter are mentioned in Table A4.

Table 5. Characteristics of the testing inverter.

V_{DC}, V	F_{sw}, kHz	F_{fund}, kHz	Load (per Phase)	Θ_{hs-amb}, $\frac{K}{W}$	Θ_{c-hs}, $\frac{K}{W}$
350	50	1	0.5 mH, 8.6–16.8 Ohm	0.42	2.9–4

The goal of the procedure was to obtain experimental values of T_J and P_{loss} and compare them with the simulation results. The system parameters from Table 5 and MOSFET characteristics from Table A2 were used to simulate the performance of the test inverter using the proposed calculation model, and predict its power losses and the junction temperature. The flowchart of the experiment is presented in Figure 19. The first stage was required to create a valid and accurate temperature scale of the MOSFET's junction temperature T_J. The temperature sensor was located on the top surface of the MOSFET's case; therefore, it measured temperature T_{C1} close to the virtual case temperature T_C.

The connection of the experimental setup for both parts of the test is presented in Figure 20. During the first part, the DC power supply worked in current control mode, and only Q3 conducted. The drain-source voltage V_{DS} was measured with high accuracy at source and drain pins of the MOSFET were measured using a voltmeter with a large averaging period. The temperature sensors were K-type thermocouples attached to the MOSFETs and heatsink surfaces using thermal conductive material. A photo of the test inverter is demonstrated in Figure 21.

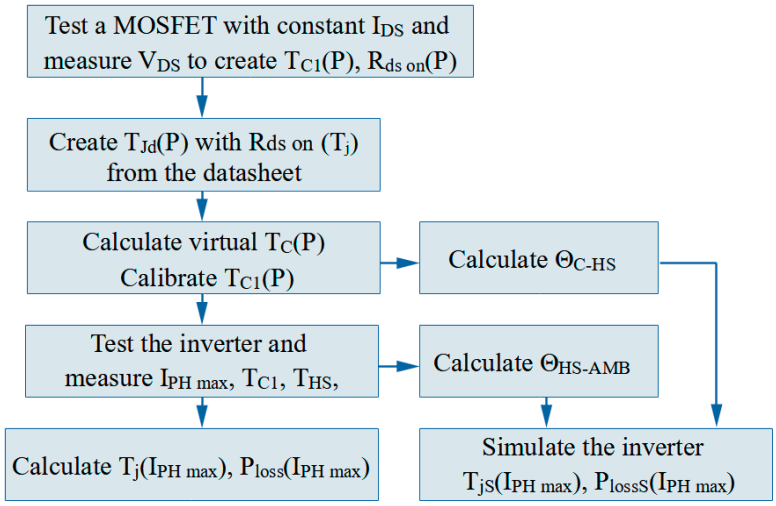

Figure 19. Algorithm of the experiment to obtain T_J and P_{loss}.

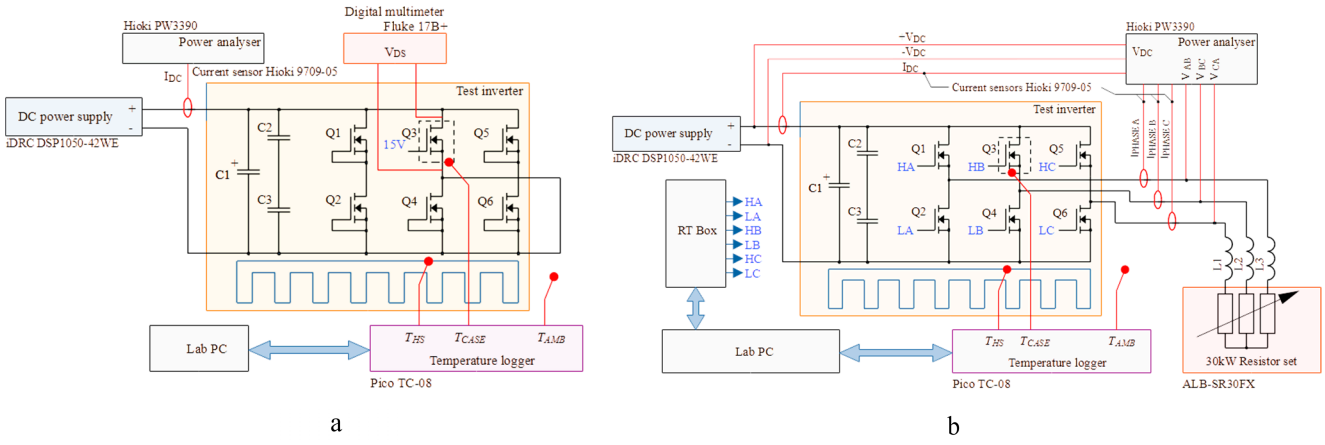

Figure 20. Test setup for Rds measurements (**a**) and 3-phase inverter operation (**b**).

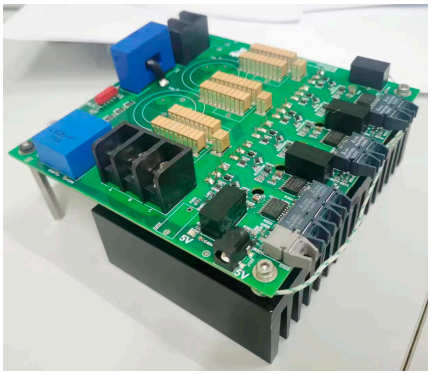

Figure 21. Test inverter for the experiment setup.

The junction temperature T_J and P_{loss} could be evaluated with high accuracy in this stage due to the high temperature coefficient of resistance, stable value of direct current and precise voltage measurement. In Figure 22a, a curve of the datasheet-based junction temperature T_{Jd} indicates values that were calculated according to MOSFET's channel active resistance. The temperature difference between T_{Jd} and the case temperature should be equal to $\Theta_{J-C} \cdot P_{loss}$; however, the results show that the measured case temperature T_{C1} had an additional constant offset of 15 °C. The proposed method (i.e., $T_J = T_{C1} + \Theta_{J-C} \cdot P_{loss} + 15$ °C) of junction temperature evaluation fitted the curve of T_{Jd} starting from $T_J = 70$ °C (see

Figure 22). For lower junction temperatures the accuracy was not high enough due to the flat shape of $R_{ds\ on}(T_J)$.

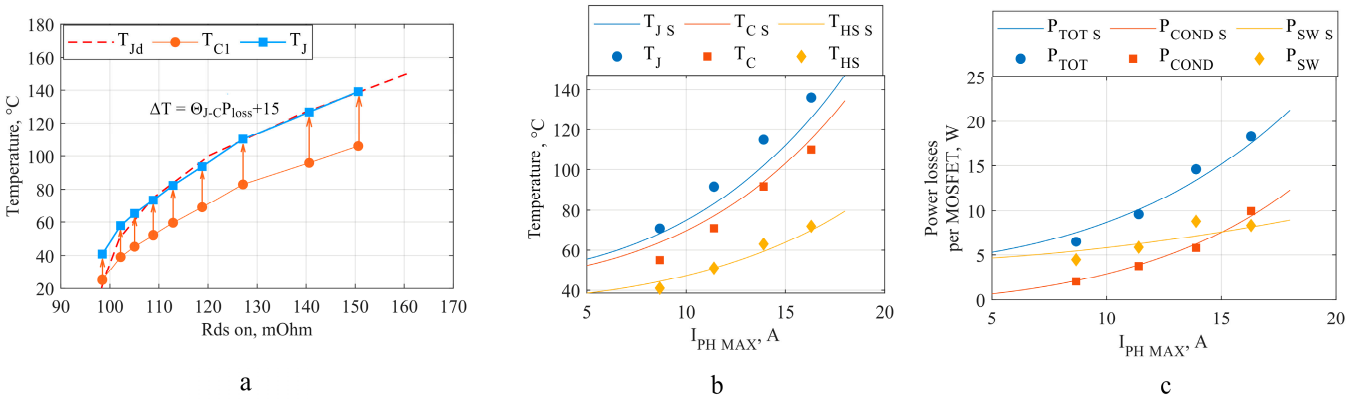

Figure 22. Experimental results: (**a**) calibration of T_C measurement at 1st stage; (**b**) comparison between predicted and measured temperatures (junction, case and heatsink); (**c**) comparison between predicted and measured power losses for a MOSFET (total, conduction and switching).

The results of the simulation (simulated junction temperature T_{JS}, simulated case temperature T_{CS}, simulated heatsink temperature $T_{HS\ S}$, simulated total losses $P_{TOT\ S}$, simulated conduction losses $P_{COND\ S}$, simulated switching losses $P_{SW\ S}$) are demonstrated in Figure 22b,c together with the experimentally obtained values. According to the results of the given experiment, the proposed thermal model demonstrated accuracy in power losses and junction temperature.

5. Discussion

According to the analysis results, discrete components can compete with power modules in terms of maximum output power and ability to operate under high ambient temperature. The requirements for the maximum case temperature significantly limit power modules in HT operations, and discrete components are free from such restrictions. Although a small size of packages does not lead to a guaranteed advantage in the inverter's area or volume, the higher weight of power modules still might be considered a severe drawback in some applications.

THT devices are the best replacement for power modules in high-power inverters in most cases. In contrast to SMT MOSFETs, THT devices demonstrate low conduction losses for the 1200 V series, which is important for EV applications.

SMT devices showed a higher efficiency and compatible output current, but they were unable to reach the same power levels primarily due to the lower drain voltage. The available SMT packages suffer from the small area of thermal pads and the unavoidable presence of a PCB insulation layer. At some point, the higher number of MOSFETs in parallel cannot increase the output power because of the increased switching losses. It would be more reasonable to use these devices in applications with limited space or specific design constraints (for instance, small PCB area or the need to use PCB as a heatsink) than as a direct alternative to power modules.

In general, several devices in SMT and THT had close results, so they can be easily replaced by each other. This fact gives an obvious advantage in terms of flexibility of component selection and their availability. Manufacturers constantly modify and enhance switches by adding new features (for instance, embedded insulation for TO-247) or increasing commutating capabilities. Nevertheless, one should remember to maximize the equality in current sharing using layout symmetry and reserve a safe margin of junction temperature to compensate for a deviation in MOSFET parameters.

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Appendix A

Table A1. List of SMT MOSFETs.

№	Name	Year	$R_{ds\ on}$, mOhm	$I_{dc\ max}$, A	V_{dc}, V	Θ_{J-C}, K/W	C_{ISS}, nF	T_J, °C	A_{HS}, mm^2	Package	Manufacturer
1	SCTL90N65G2V	12.2020	18	40	650	0.16	3.38	175	31.7	PowerFLAT 8 × 8	ST Microelectronics
2	SCT011H75G3AG	3.2022	11	110	750	0.23	3.83	175	53.3	H2PAK-7	
3	SCTH70N120G2V-7	8.2020	21	90	1200	0.32	3.54	175	53.3	H2PAK-7	
4	AIMBG120R010M1	3.2023	8.7	205	1200	0.13	5.7	175	49.3	PG-TO263-7-HV-ND5.8	Infineon
5	UJ4SC075005L8S	2.2023	0.005	120	750	0.1	8.37	175	76.6	MO-229	UnitedSiC
6	G3R30MT12J	11.2020	30	85	1200	0.3	3.86	175	44.6	TO-263-7	GeneSiC
7	NTBL045N065SC1	4.2022	33	73	650	0.43	1.87	175	55.2	H−PSOF8L	Onsemi
8	NVBG015N065SC1	2.2021	12	145	650	0.3	4.69	175	52.0	D2PAK−7L	
9	NVBG020N090SC1	8.2019	20	112	650	0.31	4.42	175	52.0	D2PAK−7L	
10	NTBG014N120M3P	4.2022	16	104	900	0.33	6.31	175	52.0	D2PAK−7L	
11	SCT4013DW7	3.2023	13	98	750	0.43	5.48	175	65.5	D2PAK-7	Rohm
12	SCT4018KW7	3.2023	18	75	1200	0.43	4.53	175	65.5	D2PAK-7	

Table A2. List of THT MOSFETs.

№	Name	Manufacturer	Year	$R_{ds\ on}$, mOhm	$I_{dc\ max}$, A	V_{dc}, V	C_{ISS}, nF	Q_g, µC	Θ_{J-C}, K/W	T_J, °C	Package
1	P3M12017K4	PNJ semi	6.2021	17	151	1200	7.29	0.27	0.19	175	TO-247-4
2	C3M0016120K	Wolfspeed	4.2019	16	115	1200	6	0.21	0.27	175	TO-247-4
3	IMZA120R007M1H	INFINEON	1.2022	7	225	1200	9.17	0.22	0.15	175	PG-TO247-4-STD-T3.7
4	UF3SC120009K4S	UnitedSiC	12.2019	8.6	120	1200	8.5	0.23	0.15	175	TO 247-4L
5	UJ4SC075006K4S		7.2021	5.9	120	750	8.31	0.16	0.16	175	TO 247-4L
6	NTH4l015N065SC1-D	onsemi	4.2021	12	142	650	4.79	0.28	0.3	175	TO 247-4L
7	G3R20MT12K	GeneSiC	1.2023	12	155	1200	9.34	0.28	0.26	175	TO 247-4
8	NTH4L014N120M3P	onsemi	1.2023	14	127	1200	6.23	0.33	0.17	175	TO 247-4L
9	MSC015SMA070B4	Microsemi		15	140	700	4.5	0.22	0.22	175	TO 247-4L
*	C2M0080120D	Wolfspeed	2013	80	36	1200	1.13	0.071	0.6	150	TO 247

* only for experimental validation.

Table A3. List of power modules.

№	Name	Year	$R_{ds\ on}$, mOhm	$I_{dc\ max}$, A	V_{dc}, V	C_{ISS}, nF	Q_g, µC	Θ_{J-C}, K/W	T_J °C	Length, mm	Width, mm	Height, mm	Weight, g
1	CAB760M12HM3	2.2022	1.33	1015	1200	79.4	2.72	0.068	175	110	65	12.2	180
2	CAB530M12BM3	3.2021	2.67	719	1200	39.6	1.36	0.065	175	103.5	60.4	30	300
3	CAB450M12XM3	6.2019	2.6	450	1200	38.0	1.33	0.11	175	80	53	15.75	175
4	MSCSM120AM02CT6LIAG	1.2020	2.1	947	1200	36.2	2.78	0.04	175	108	62	16	320
5	MSCSM120TAM11CTPAG [1]	1.2020	8.4	251	1200	9	0.69	0.144	175	108	62	11.5	250
6	GE12047CCA3	5.2021	3.1	475	1200	29.3	1.25	0.1	175	89.3	51.2	14.8	120
7	FS03MR12A6MA1B [1,2]	4.2021	2.75	400	1200	42.6	1.32	0.115	150	154	95	19	720

[1]: 3-phase module, [2]: designed for direct cooling.

Table A4. Components of the test inverter.

Component Function	Component Type	Notes
Input capacitor	MAL205737101E3 (100 µF 450 V), 2 in parallel B58035U5106M001 (10 µF 500 V), 3 in parallel	C1 C2, C3
Gate drivers	1ED3320MC12N	
Power switches	C2M0080120D	Q1–Q6
DC-link snubber capacitor	B32714H1205K000 (2 µF 1100 V) and B58035U9504M (500n 900 V) in parallel	

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