Low-Density Parity-Check Codes for Asymmetric Distributed Source Coding

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Abstract—Low-Density Parity-Check (LDPC) codes achieve good performance, tending towards the Slepian-Wolf bound, when used as channel codes in Distributed Source Coding (DSC). Most LDPC codes found in literature are designed assuming random distribution of transmission errors. However, certain DSC applications can predict the error location within a certain level of accuracy. This feature can be exploited in order to design application specific LDPC codes to enhance the performance of traditional LDPC codes.

This paper proposes a novel architecture for asymmetric DSC where the encoder is able to estimate the location of the errors within the side information. It then interleaves the bits having a high probability of error to the beginning of the codeword. The LDPC codes are designed to provide a higher level of protection to the front bits. Simulation results show that correct localization of errors pushes the performance of the system on average 13.3% closer to the Slepian-Wolf bound, compared to the randomly constructed LDPC codes. If the error localization prediction fails, such that the errors are randomly distributed, the performance is still in line with that of the traditional DSC architecture.

Keywords-LDPC codes; Distributed Source Coding (DSC); Slepian-Wolf theorem

I. INTRODUCTION

In asymmetric Distributed Source Coding (DSC) two correlated sources X_i and Y_i are encoded separately and then jointly decoded to achieve compression. A schematic diagram of the traditional asymmetric DSC architecture is shown in Fig.1, where source X_i exploits its own correlation to minimize the average number of bits per source symbol, up to the entropy measure $H(X_i)$. On the other hand, source Y_i, is encoded using the Slepian-Wolf theorem, where the decoder predicts the input Y_i, by interpolating/extrapolating source X_i, and uses it as side information (SI) to achieve lossless compression of the source Y_i. Slepian and Wolf proved that lossless compression of Y_i can be achieved with an arbitrary small probability of reconstruction error, at rates approaching the conditional entropy $H(Y_i|SI_i)$ [1].

Later Wyner proposed that the side information SI_i can be considered as a corrupted version of Y_i and therefore compression can be achieved through robust channel codes [2]. In this architecture, Y_i is compressed into its syndrome representation S. At the decoder, the side information SI_i is then used to distinguish Y_i from among the other coset elements represented by the same syndrome S. Sophisticated channel codes such as Turbo codes [3] – [5], Low Density Parity Check (LDPC) codes [6] and their rate-adaptive counterparts: LDPC Accumulate (LDPCA) codes and Sum LDPCA (SLDPCA) have been used in the past as channel codes to approach the Slepian-Wolf bound, with LDPCA and SLDPCA codes performing best [7].
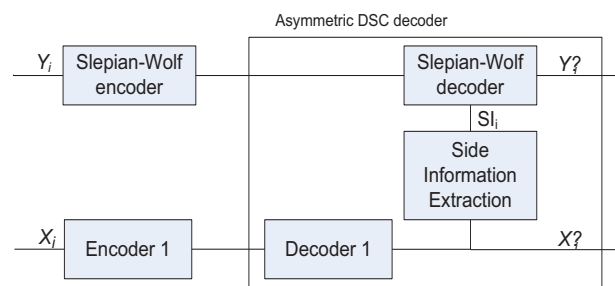

Figure 1.   The Asymmetric Distributed Source Coding (DSC) Architecture

Traditional LDPC code implementations assume that the errors between the SI_i and Y_i are randomly distributed. However, in some practical implementations of DSC, the location of the corrupted bits can be predicted to a certain extent, thus making standard LDPC implementations sub-optimal for these applications.

This paper presents a modification in the traditional DSC architecture, where the bits having a higher probability of error are localized and interleaved to the beginning of the codeword. Such knowledge is then assumed at the design of the LDPC codes, which are thus optimized to give a higher level of protection to the bits found at the beginning of the codeword. Simulation results demonstrate that the performance of the proposed architecture approaches the Slepian-Wolf bound to 6.2% at low rates and 9.3% at high rates. Hence, these codes outperform all the regular LDPC codes found in literature when the error locations are approximated correctly. Furthermore, if the error distribution is not accurately predicted, the system is designed such that, at worst, it performs as the traditional DSC schemes.
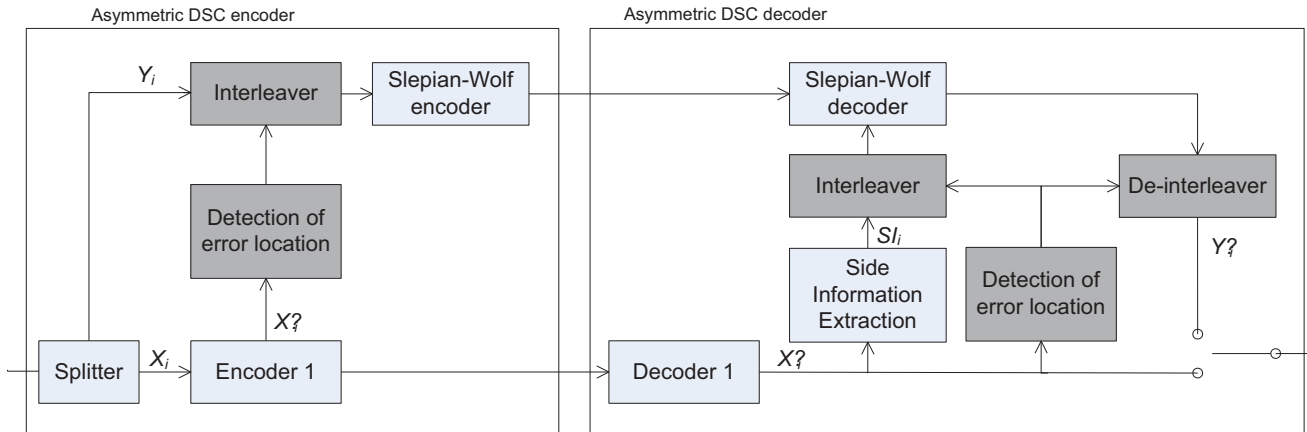
Figure 2. Proposed Architecture for Asymmetric DSC with the Additional Blocks Highlighted.

The paper is organized as follows: Section II discusses the proposed DSC architecture and the suitability of channel codes with Unequal Error Protection (UEP) for the new architecture. Section III introduces new features that can be considered to enhance the performance of LDPC codes for non-uniform channels while the following section considers the algorithms used to construct such codes. The performance of the proposed solution is then evaluated in Section V. Finally, section VI concludes the paper.

II. PROPOSED ASYMMETRIC DISTRIBUTED SOURCE CODING ARCHITECTURE

Asymmetric DSC systems generally assume that the errors between Y_i and SI_i are uniformly distributed across the whole codeword. This assumption is valid for traditional communication systems. However in some practical implementations, such as Distributed Video Coding (DVC) and Sensor Networks, the errors in the SI can be predicted with a certain level of confidence [8]. This suggests that the *dependency channel*, modeling the correlation between Y_i and SI_i, should not be considered as having a uniform probability of error. It should rather be considered as a channel with a higher probability of error in areas having low side information reliability. Hence, channel codes with Unequal Error Probability (UEP) can be used to improve the performance of the Slepian-Wolf codec.

A potential issue with this approach is that the error profile of the *dependency channel* varies continuously since the location of the error between Y_i and SI_i is dynamic. Fig. 2 illustrates the architecture that is proposed to deal with this issue. In this architecture, the Slepian-Wolf encoder uses sequence X'_i (a copy of the decoded quantized sequence expected at the output of the decoder) to predict the reliability of the side information bits. It then interleaves the bits corresponding to the low reliability areas at the beginning of the codeword. At the decoder, the same sequence X'_i is used to determine the interleaving sequence

used at the encoder. This is used to synchronize the bits of sequence SI_i with those of the original source Y_i. A de-interleaving sequence is also determined at the decoder and used to shift the decoded bits back to their original position generating the correct output sequence. Using this idea, the bits having a higher probability of error are always expected at the beginning of the codeword. The designed LDPC codes are optimized for such error pattern, yet it is also desirable if their performance does not degrade when the error location prediction fails.

III. LDPC CODE CONSTRUCTION

The design of traditional LDPC codes is understood as a problem of finding the correct degree distribution using density evolution curves [9]-[11]. The edges are then placed at random using graph conditioning techniques, such as the Progressive Edge-Growth (PEG) algorithm [12], in order to obtain the largest cycles possible and improve iterative decoding.

To design UEP LDPC codes, the authors in [10] exploited the natural UEP property of irregular LDPC code, where the higher degree variable nodes are known to converge faster than the lower degree variable nodes. They have adapted the degree distribution of the variable nodes to protect part of the codeword more than the rest. However, they still assumed a uniform channel and distributed the edges randomly across the whole codeword.

This paper considers a new approach to design regular LDPC codes having good performance in channels with non-uniform error distribution. It is proposed that after obtaining the degree distributions, the variable nodes connected to the check nodes are not selected completely at random. The connection of the check nodes' edges should be biased such that each check node is connected to more variable nodes having a low probability of error. This concept is demonstrated in Fig. 3, where the code construction of a rate- ½ (18, 9) code having a regular degree distribution of 3 ($\lambda(x) = \rho(x) = x^2$) is considered. The

variable nodes representing low reliability bits are placed on the left hand side. It can be clearly seen that in this code construction, each check node receives at most one unreliable edge at a time, thus hypothetically improving the error correction capabilities of the LDPC codes.
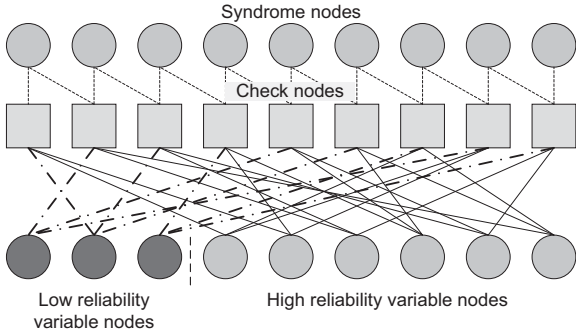

Figure 3.   Construction of a rate-1/2 (18,9) code.

The log-likelihood ratios given by each check node have a higher probability of error correction since most of the input come from reliable variable nodes. The unreliable bits receive extrinsic information from reliable variable nodes improving the convergence of the LDPC and hence for a given number of iterations it can correct more errors. Note that the variable nodes connected to each check node are still selected at random from the remaining variable nodes having a high/low probability of error. With this element of randomness it is expected that if detection fails, the performance of the code falls back to that of a randomly constructed code having the same degree distribution.

IV.   CONSTRUCTION OF THE RATE ADAPTIVE LDPC CODES

The Slepian-Wolf codec achieves compression through rate-adaptive codes. Rate-adaptive LDPC codes, called LDPCA codes, were considered in [7], where the authors proposed LDPC codes consisting of LDPC syndrome-former concatenated with an accumulator. These codes achieve compression by merging the check nodes until the required compression ratio is achieved.

Following the discussions in the previous section, it is proposed that the construction of the LDPCA code is biased such that every check node has more than half of the edges connected to the part of the codeword having a low probability of error. This paper considers only the construction of regular-3 degree LDPC codes. Hence every check node should be connected to at most one variable node having a high probability of error.

Optimal decoding of LDPC codes can be achieved only in cyclic-free graphs [13]. Hence, graph conditioning techniques, such as those in [12], are considered during code construction, to increase the length of the cycles. However, since the graph becomes denser at lower rates, it becomes difficult to consider conditioning techniques for all the lower rate sub-codes. For this reason, graph conditioning is considered only for the base code, with a compression ratio 1:1, as proposed in [14]. Nevertheless for all the lower rate sub-codes, harmful structures such as 4-length cycles are prevented from affecting the first part of the matrix, where errors are more likely to occur. Furthermore, the graph structure is ensured to be valid for all rates by guaranteeing that no edges are lost over several merging steps [7]. This implies that check nodes that require to be merged are forbidden to have a common neighbor.

V.   EXPERIMENTAL RESULTS

The performance of the proposed architecture, using the regular 3-degree LDPCA code designed in Section IV, is considered in Fig. 4. The results obtained are compared with the performance of the traditional architecture using the latest LDPC codes designed for DSC applications, such as: the regular LDPCA codes in [7], the irregular LDPCA in [15], and Sum LDPCA (SLDPCA) codes [7]. The performance profiles obtained by each solution are also shown in Fig. 4.
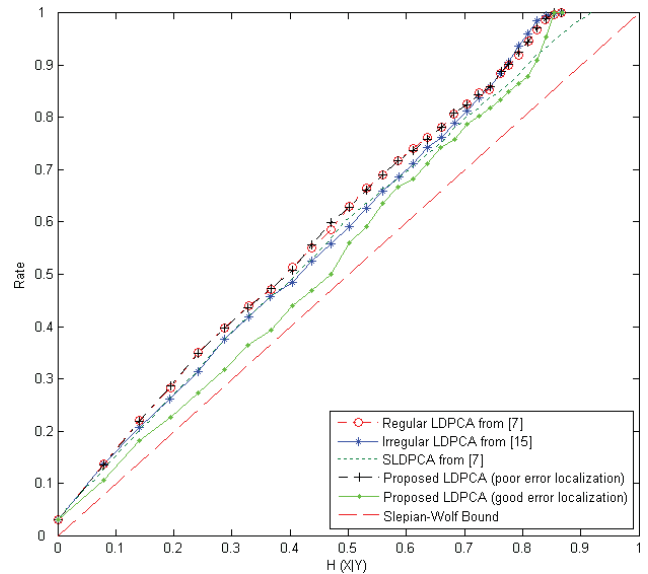

Figure 4.   Performance obtianed using different channel codes.

The irregular LDPCA code has a degree distribution of ($\delta_2 = 0.321$, $\delta_3 = 0.456$, $\delta_6 = 0.01$, $\delta_7 = 0.174$, $\delta_8 = 0.039$), while the SLDPCA code has a degree distributions of ($\delta_2 = 0.3$, $\delta_3 = 0.4$, $\delta_4 = 0.3$). In all cases, the code has a codeword length of 396 bits and a rate multiple of 66, with the lowest rate being 2/66. For each packet of parity bits, the decoder tries to correct the errors in the side information for a maximum of 50 iterations, before requesting additional parity information. An average of 100 rates was considered for every entropy point.

It can be immediately noticed that, if the prediction of the error location is not accurate, the performance of the

system does not drop below that of the traditional architecture with regular LDPCA codes. Therefore, the proposed biasing, done on the check nodes' edges, did not affect the capability of the code to correct random errors. This guarantees that under worst case conditions the proposed system will not perform worse than the traditional architecture.

The results further demonstrate that if the encoder manages to detect correctly the location of almost all the errors in the side information, the proposed architecture performs closer to the Slepian-Wolf bound. It can approach the bound up to 6.2% at low rates, and 9.3% at high rates; operating on average 9.6% closer to the bound compared to the irregular LDPCA and 13.3% closer than the regular LDPCA. Thus, the proposed LDPCA codes manage to consistently outperform even the irregular LDPCA codes and irregular SLDPCA codes proposed in [7].

VI. Conclusion

This paper presented a new architecture that can be used for asymmetric DSC, where the encoder predicts the reliability of the side information bits and interleaves the bits having high probability of error to the beginning of the codeword. This paper further presents a novel approach in designing LDPCA codes optimizes for such error patterns. Simulation results have shown that the proposed scheme outperforms all the other channel codes considered in this paper when the errors are correctly located. Moreover, in the worst case scenario where prediction fails completely, the proposed solution is still valid since its performance becomes similar, but not worse, to the traditional architecture with the same degree distribution. Current studies are exploring the application of this solution using irregular LDPCA codes.

VII. Acknowledgment

References

[1] D. Slepian and J. Wolf, "Noiseless coding of correlated information sources," IEEE Transactions on Information Theory, vol. 19, pp. 471-480, July 1973.

[2] A. Wyner, "Recent results in the Shannon theory," IEEE Transactions on Information Theory, vol. 20, pp. 2-10, Jannuary 1974.

[3] A. Aaron and B. Girod, "Compression with side information using turbo codes," Proc. IEEE Data Compression Conf, Aug. 2002, pp. 252-261.

[4] J. Garcia-Frias and Y. Zhao, "Compression of correlated binary sources using turbo codes," IEEE Communications Letters, vol. 5, pp. 417–419, October 2001.

[5] J. Bajcsy and P. Mitran, "Coding for the Slepian-Wolf problem with turbo codes," Proc. IEEE Global Communication conference, Nov. 2001, pp. 1400-1404.

[6] A. Liveris, Z. Xiong, and C. Georghiades, "Compression of binary sources with side information at the decoder using LDPC codes," IEEE Communications Letters, vol. 6, pp. 440-442, October 2002.

[7] D. Varodayan, A. Aaron, and B. Girod, "Rate-adaptive codes for distributed source coding," EURASIP Signal Processing Journal, vol. 86, pp. 3123-3130, November 2006.

[8] R. Puri and K. Ramchandran, "PRISM: A new robust video coding architecture based on distributed compression principles," 40th Allerton Conference on communication, Control and Computing, October, Allerton, October 2002

[9] F. Cen, "Design of degree distributions for LDPCA codes," IEEE Communications Letters, vol. 13, pp. 525-527, July 2009.

[10] C. Poulliat, D. Declercq, and I. Fijalkow, "Enhancement of Unequal Error Protection Properties of LDPC Codes," EURASIP Journal on Wireless Communications and Networking, vol. 2007, pp. 1-10, July 2007.

[11] T. Richardson and R. Urbanke, "The capacity of low-density parity-check codes under message-passing decoding," IEEE Transactions on Information Theory, vol. 47, no. 2, pp. 599-618, February 2001.

[12] E. Eleftheriou and D. Arnold, "Regular and irregular progressive edge-growth tanner graphs," IEEE Transactions on Information Theory, vol. 51, pp. 386-398, January 2005.

[13] R. M. Tanner, "A recursive approach to low complexity codes," IEEE Transactions on Information Theory, vol. IT-27, no. 6, pp. 533-547, September 1981.

[14] J. Ascenso, C. Brites, and F. Pereira, "Design and performance of a novel low-density parity-check code for distributed video coding," Proc. IEEE International Conference on Image Processing, Oct. 2008, pp. 1116-1119.

[15] Rate-Adaptive LDPC Accumulate Codes for Distributed Source Coding. [Online] available: http://ivms.stanford.edu/~varodayan/ldpca.htm